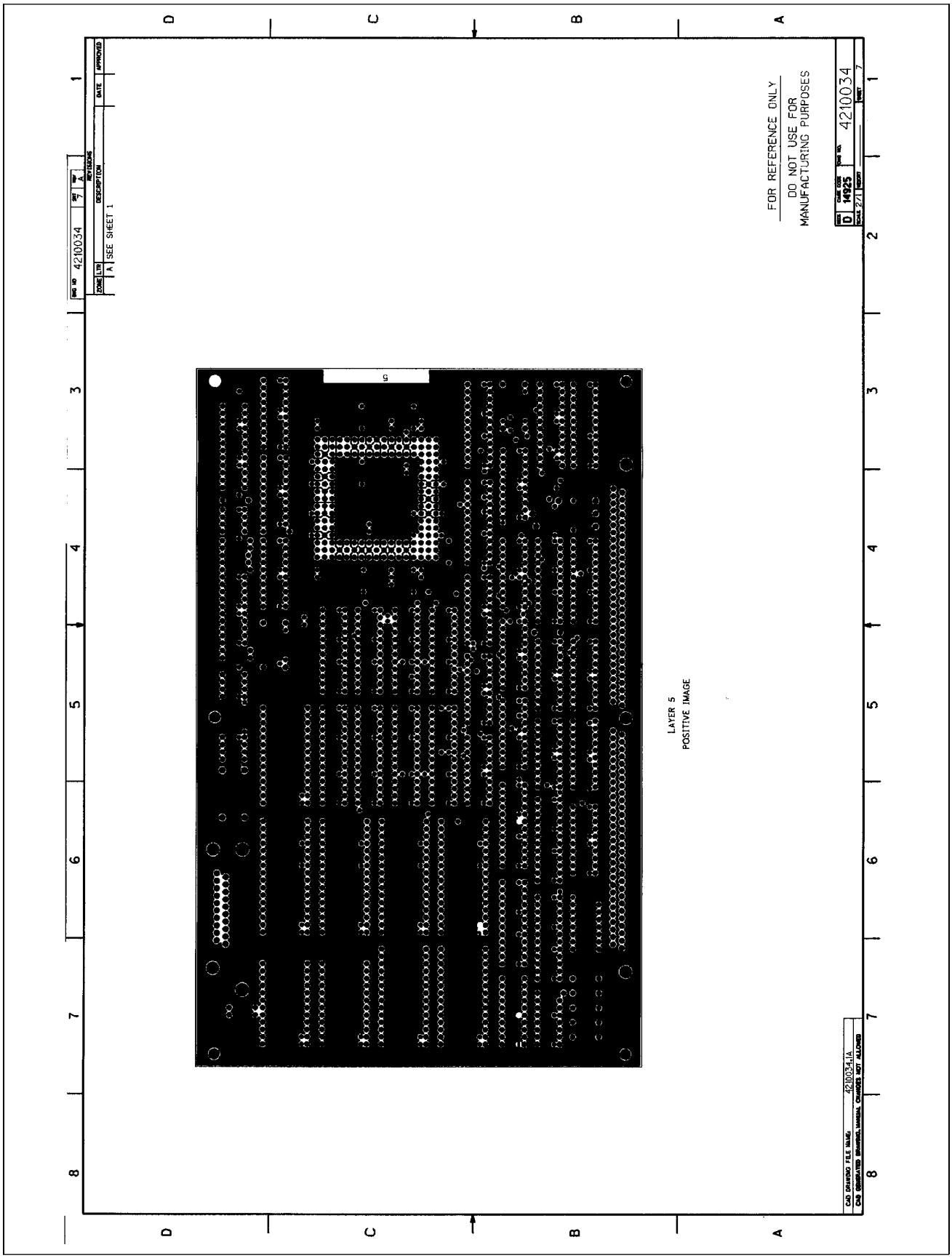

Figure 5–3 Typical Multilayer Master Drawing with External Heatsink, Sheet 7 of 14

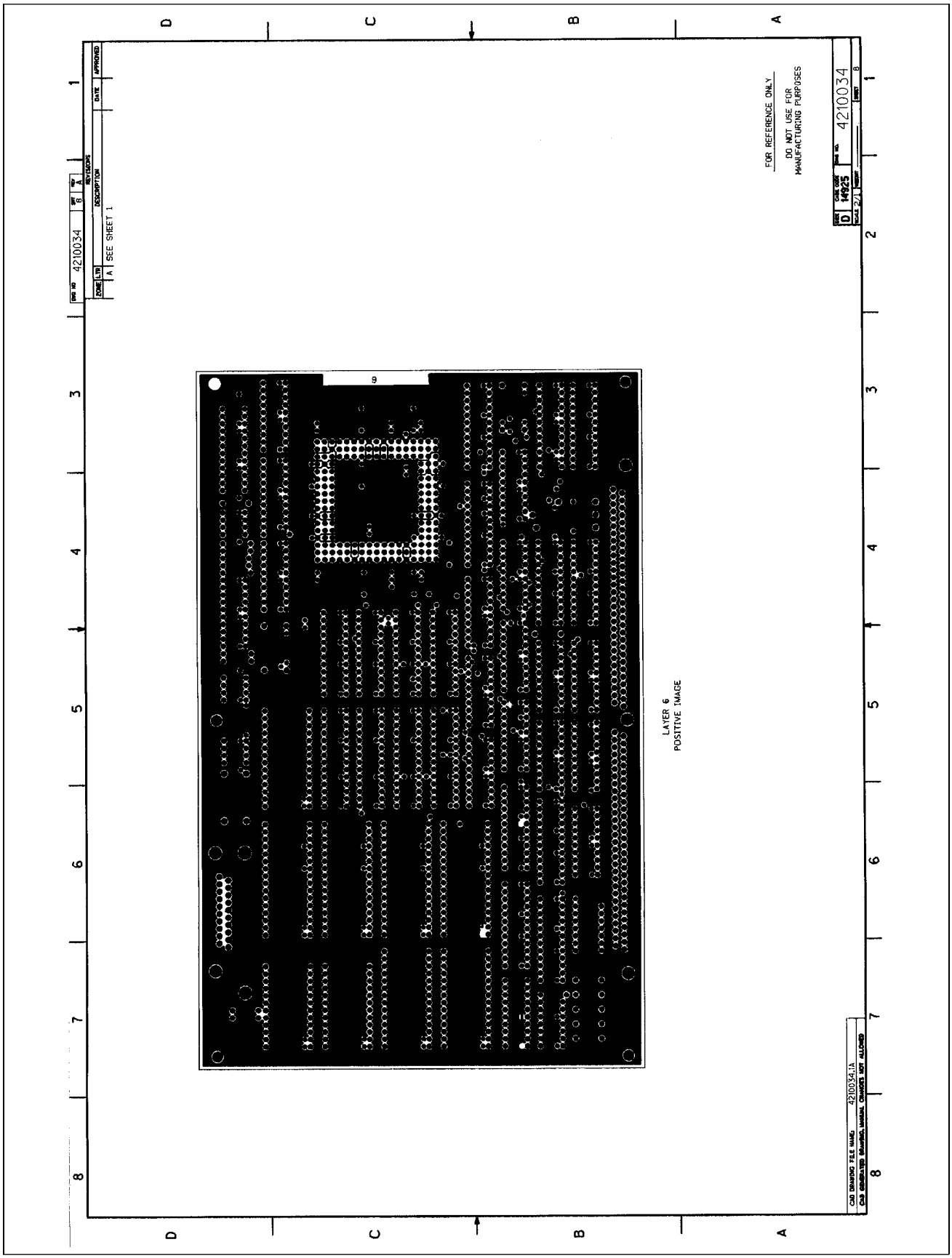

Figure 5–3 Typical Multilayer Master Drawing with External Heatsink, Sheet 8 of 14

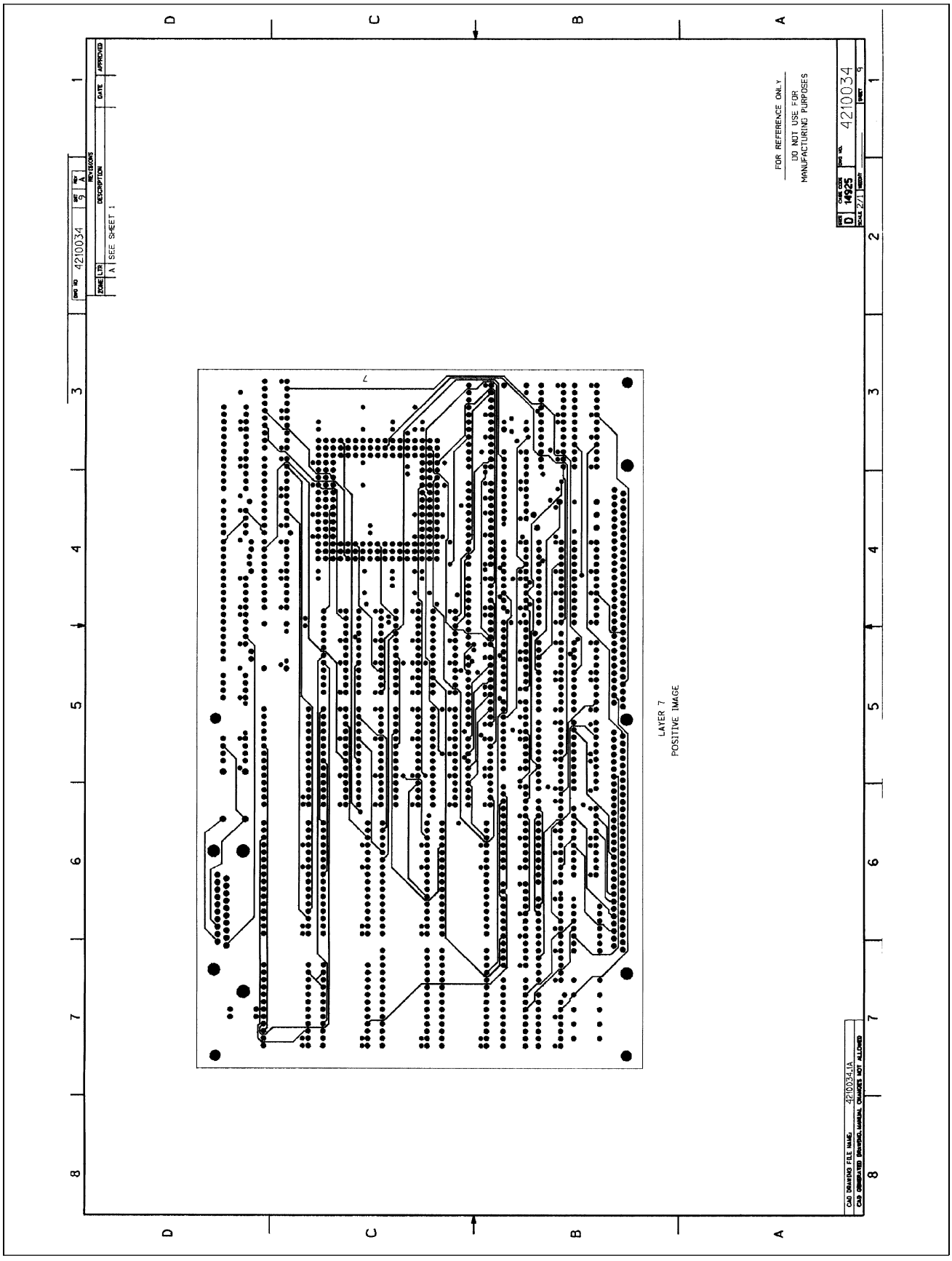

Figure 5–3 Typical Multilayer Master Drawing with External Heatsink, Sheet 9 of 14

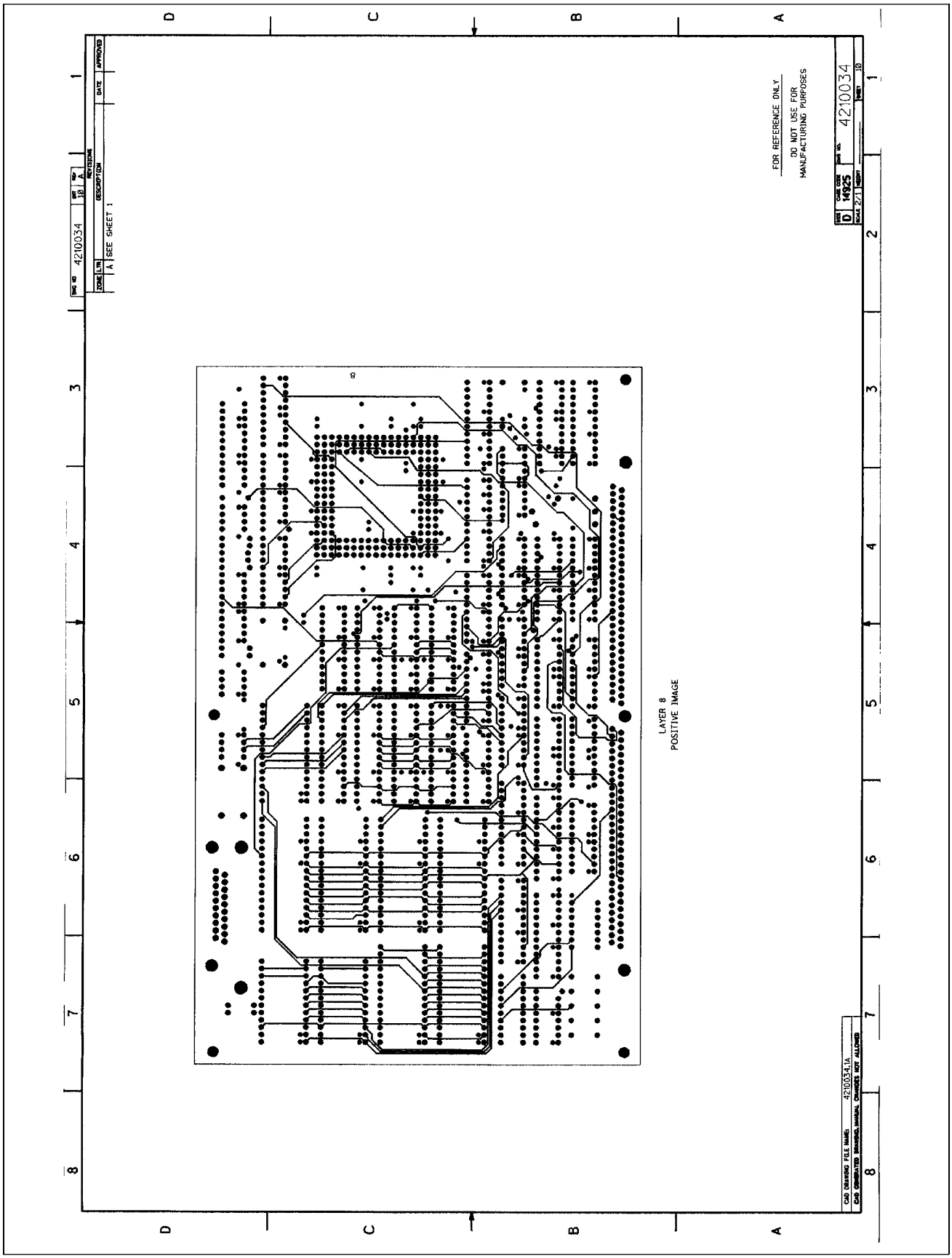

Figure 5–3 Typical Multilayer Master Drawing with External Heatsink, Sheet 10 of 14

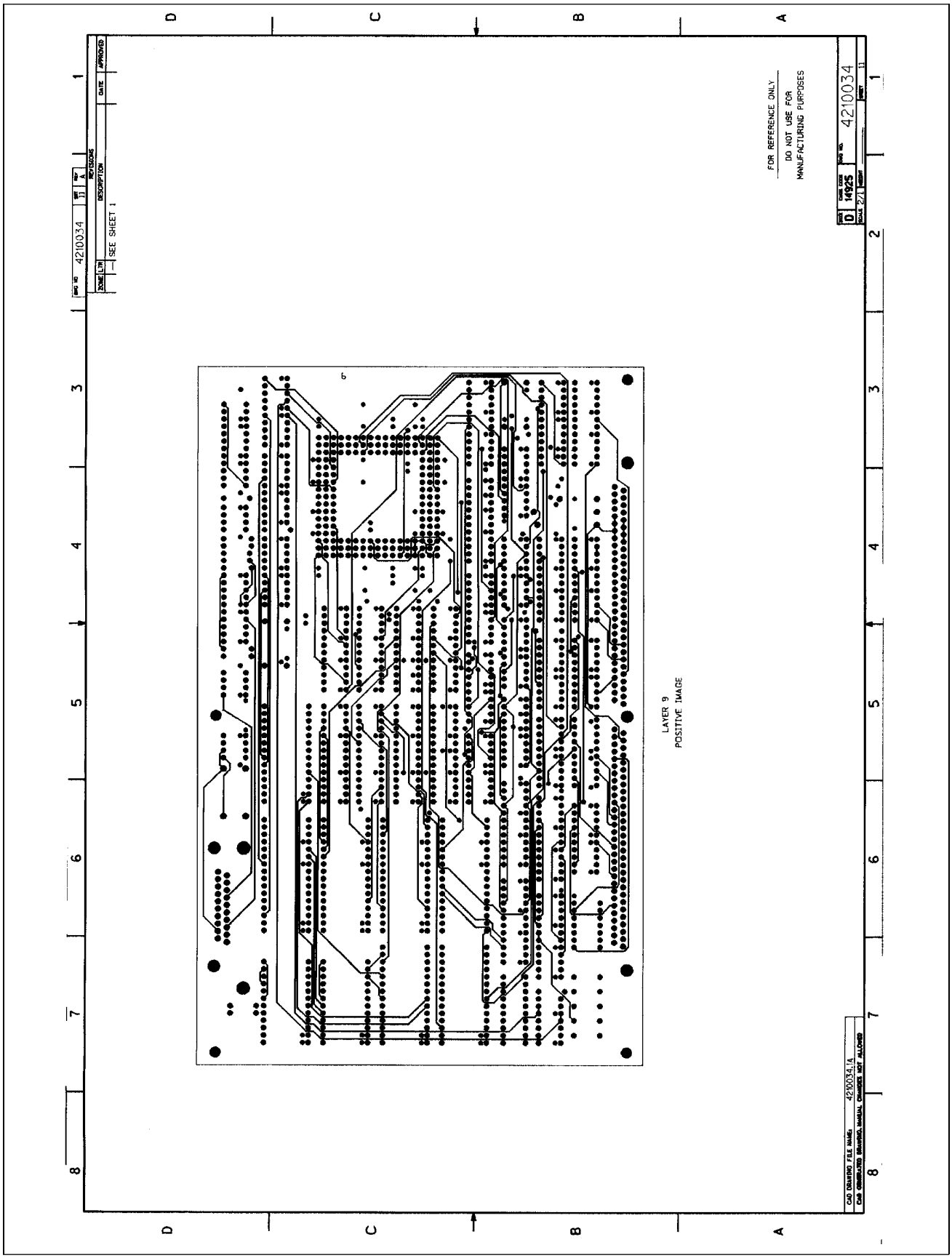

Figure 5–3 Typical Multilayer Master Drawing with External Heatsink, Sheet 11 of 14

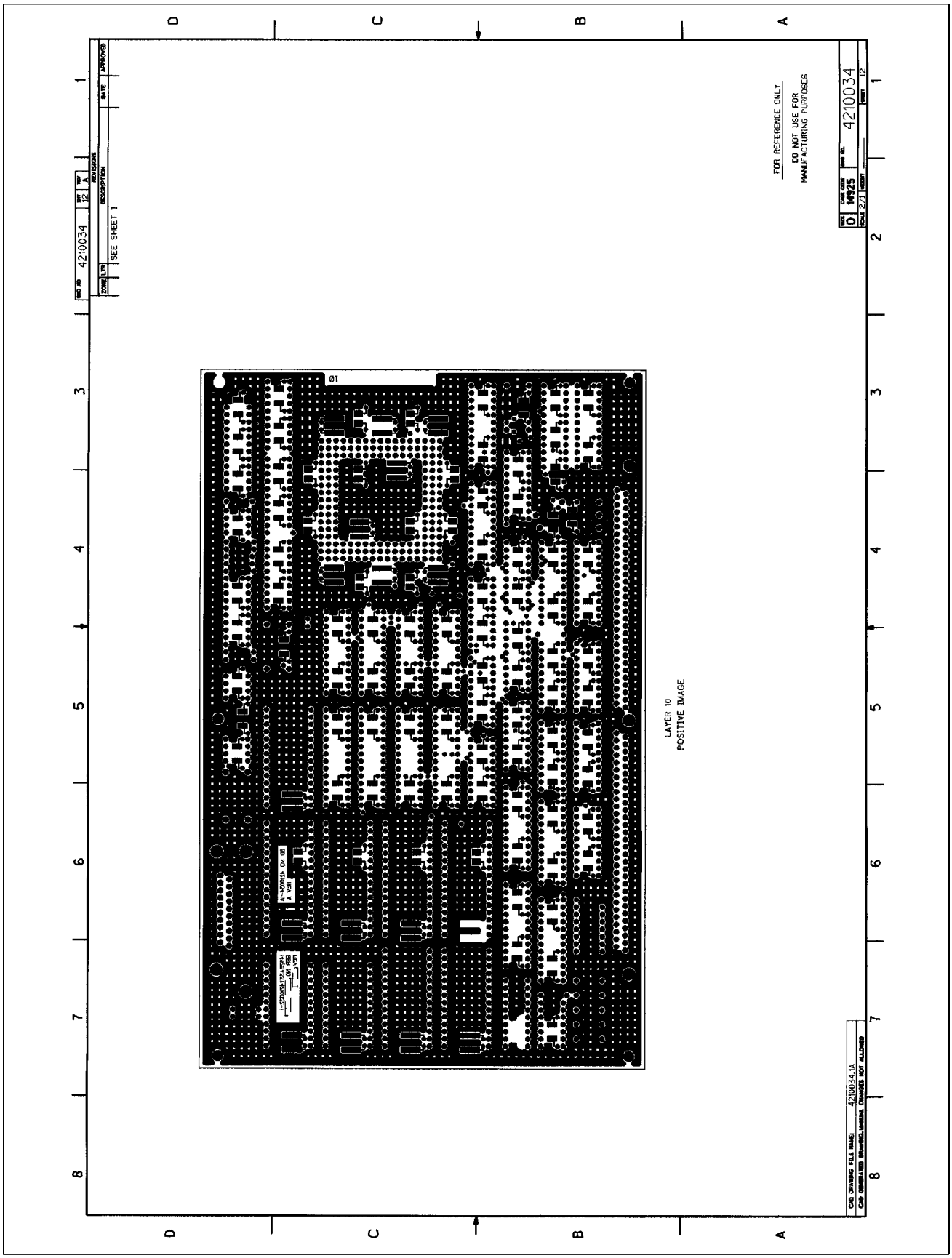

Figure 5–3 Typical Multilayer Master Drawing with External Heatsink, Sheet 12 of 14

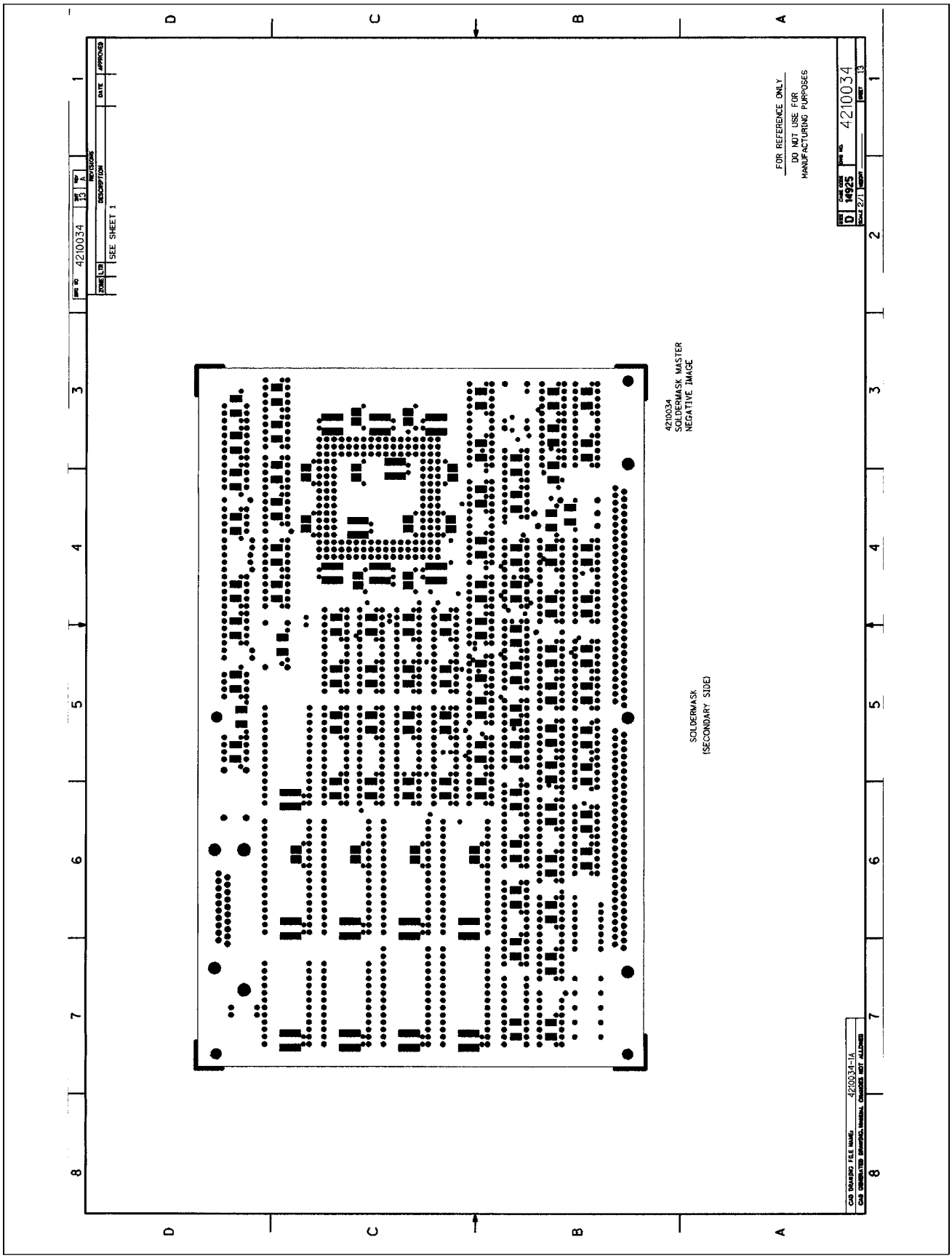

Figure 5–3 Typical Multilayer Master Drawing with External Heatsink, Sheet 13 of 14

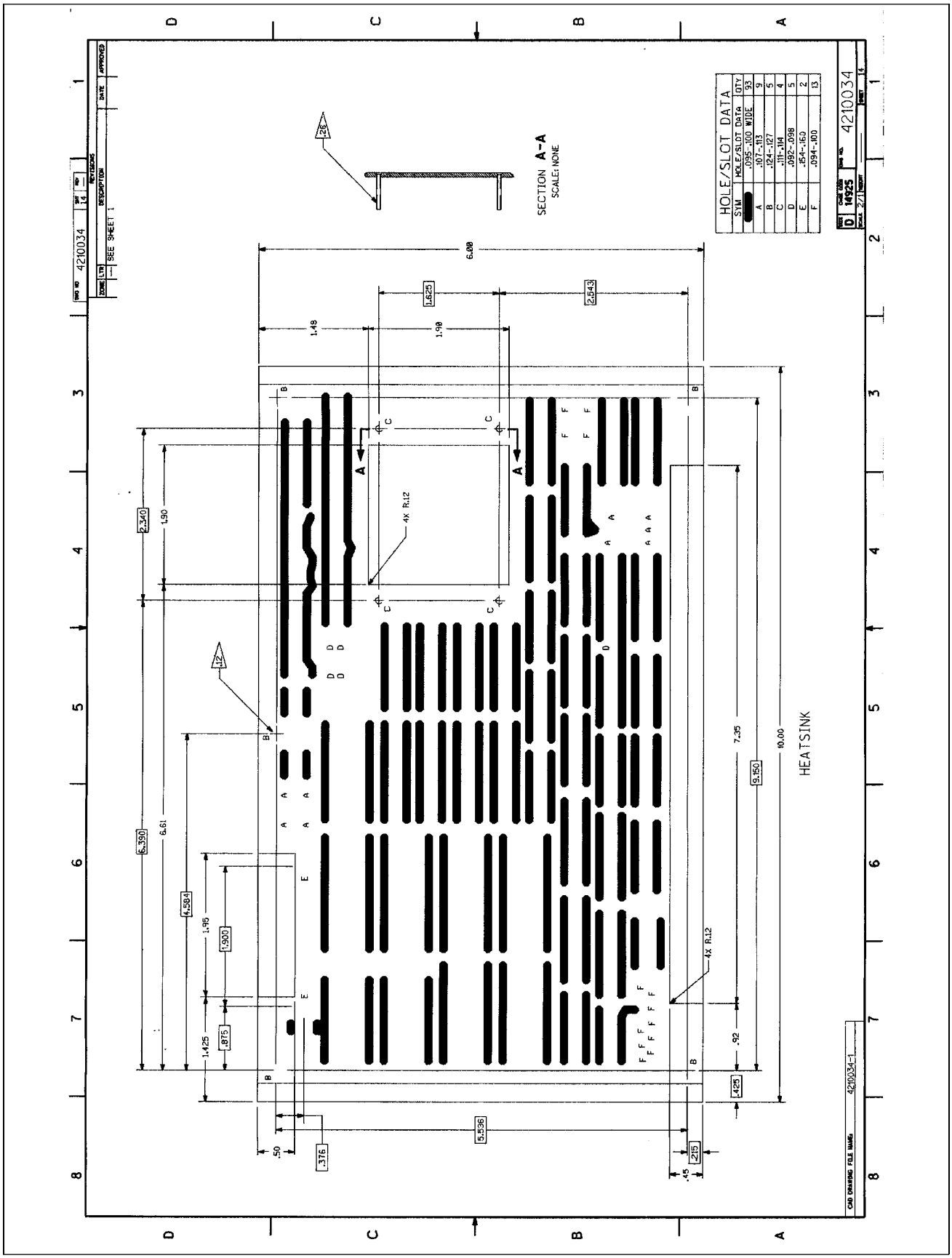

Figure 5–3 Typical Multilayer Master Drawing with External Heatsink, Sheet 14 of 14

6.0 MASTER DRAWING NOTES AND CHECK LIST

6.1 Examples of Typical Notes:

1. Fabricate boards in accordance with IPC-RB-276, Class 3. Finished boards must meet quality conformance testing and inspection as specified.

*2. Material in accordance with MIL-S-13949/4, laminated sheet, HTE copper-clad, type GF glass cloth base, flame resistant (meeting UL 94V-1 or better). Tg rating: 140 to 160°C.

*3. Material in accordance with MIL-S-13949/12, plastic sheet, type GF base material, glass base preimpregnated (B-stage), Tg rating: 140 to 160°C.

*4. Board fabricator **shall** apply date code, fabricator's cage code, I.D. and UL marking to primary side and secondary side where indicated. Marking to be copper etched.

*5. Construction to be solder mask over bare copper (SMOBC), using Type XXXX, photoimageable dry film, 0.003 in thick. Apply to primary and secondary sides in accordance with IPC-SM-840, (type B, Class 3). Use appropriate solder mask artwork for each side of board. Puncturing of tented holes is not permissible.

*6. Solder mask misregistration **shall** not exceed +0.004 in. Solder mask overlap permitted on circular lands only, and **shall** not exceed 0.001 in. No overlap permitted on SMD rectangular lands.

*7. Solder mask thickness: 0.002 in min./0.003 in max. Solder mask material to be light green in color and highly transparent.

8. Drill boards using drill data, drill pattern and hole schedule. Hole locations may vary within .004 in (Radial Error) max. about true position.

9. All holes are plated-through unless noted otherwise. Minimum copper plating in plated holes to be .001 in. Copper plating in tented holes **shall** not plug holes closed.

10. Minimum annular ring:
    0.002 in minimum − external layers.
    0.001 in minimum − internal layers.

11. A certificate of compliance with IPC-RB-276, Class 3, **shall** be submitted with each lot.

12. Tin-lead plate all holes as required. Coverage and solderability **shall** meet the requirements of J-STD-001. Tented holes are not applicable.

13. Exposed lands and lines to be tin-lead coated. Tin-lead plated ''K'' holes may be reduced to the point of closure.

14. All exposed surface lands and lines to be solder coated.

15. Finished line width tolerance is +0.001 in/0.001 in (refer to chart).

16. Minimum finished spacing is 0.005 in.

17. Dimensions are after etching and plating, and are basic unless otherwise indicated.

18. Bow and twist **shall** not exceed 0.0075 inch per inch measured in accordance with IPC-TM-650, method 2.4.22.

19. All artwork or mag tape data may be adjusted by the PCB fabricator to compensate for manufacturing process tolerances. Addition of fillets at line/pad interface is preferred.

20. Land/hole fabrication allowance: 0.015 in.

*21. Silkscreen primary side (top) and secondary side (bottom) of board using white epoxy base ink per MIL-I-43553, Type II, and appropriate artwork.

*22. Test coupon: place fabricator's cage code, date code or serial no. where indicated, using white epoxy ink or copper etch. One metallographic specimen **shall** be tested and supplied with each lot of boards. A report of measurements, showing average plating thickness and quality, **shall** be supplied with each specimen. Testing **shall** include thermal stress and microsectioning per IPC-TM-650, Methods 2.1.1 and 2.6.8. Each specimen **shall** be identified and traceable back to the originating lot.

23. Bare Board Electrical Test: Bare boards **shall** be electrically tested using CAD generated net list data. This information to be supplied in IPC-D-356 format. Electrical testing **shall** follow the guidelines established by IPC-ET-652, guidelines and requirements for electrical testing of unpopulated printed boards.

Example of typical notes when using liquid photoimageable solder mask material. Notes 5, 6, and 7 may read as follows:

*5. Construction to be SMOBC, using liquid photoimageable (LPI) solder mask material, type XXXX. Apply to both external layers in accordance with IPC-SM-840, (Type B, Class 2). Use appropriate solder mask artwork for each side of board.

*6. Solder mask misregistration **shall** not exceed +/-0.004 in. Solder mask material is permitted on routing vias (J) lands only. Solder mask overlap is permitted on all other circular lands but, **shall** not exceed .001 in. No solder mask material permissible on SMD rectangular lands.

*7. Solder mask thickness: 0.0007 in min./0.002 in max. Solder mask material to be light green in color and highly transparent.

*Indicates box or flag

6.2 Master Drawing Check List The following check list is provided for the convenience of the designer assigned to review and check the completed documentation. This listing addresses those items which must be considered during the preparation of the printed board documentation package. When convenient, the requirements of the finished board may be specified in note form.

☐ Finished board specifications (e.g., IPC-RB-276) and class (e.g., Class 3) which the board fabricator must comply.

☐ Material requirements; i.e., laminate type, copper foil, U.L. requirements and Tg rating.

☐ Multilayer boards: B-stage material requirements.

☐ Board markings: consider date code, fabricator's I.D. and U.L. marking (indicate location), and marking agent (ink, copper, etc.).

☐ Construction; i.e., solder mask over bare copper (SMOBC), tin-lead plate, cap layer, etc.

☐ Solder mask material and class:
Type A, deposited image (liquid / dry);
Type B, photo defined image (liquid / dry).

☐ Solder mask thickness (min.- max.) and color.

☐ Permissible solder mask misregistration and overlap restrictions.

☐ Drilled Hole requirements:
Indicate permissible radial error about true position. Identify supported (plated) holes and non-supported holes (non-plated holes). Indicate all hole diameters (after plating) and tolerances.

☐ Copper plating thickness (minimum permissible in holes and on conductors).

☐ Indicate etchback requirements when applicable.

☐ Tin-lead plating thickness (minimum permissible: in holes and on conductors.

☐ Minimum Annular Ring requirements:
.XXX in Minimum - External Layers.
.XXX in Minimum - Internal Layers.

☐ Land / hole fabrication allowance: .XXX:.

Note: Use formula illustrated in IPC-D-275, 5.3.2.2, to calculate minimum annular ring values and fabrication allowance.

☐ Tin-lead plating requirements on surface mount lands.

☐ Nominal finished conductor (line) width: .XXX in.

☐ Finished conductor (line) width tolerance: +.XXX in / -.XXX:.

☐ Minimum finished spacing: .XXX in.

☐ Permissible bow and twist requirements; measured in accordance with IPC-TM-650, method 2.4.22.

☐ Permissible fabricator allowances:
- Artwork, mag tape data or electronic data may be adjusted by the PWB fabricator to compensate for manufacturing process tolerances.
- Addition of fillets at conductor (line) / pad interface is preferred.

☐ Indicate silkscreen ink type, when applicable.

☐ Test Coupon (quality conformance coupon) requirements:
- Indicate fabricator's test coupon requirements, per IPC-D-275, 7.0.
- Indicate marking requirements; i.e., cage code, date code, or serial number markings and locations. Indicate marking material: ink, copper, etc.

☐ Indicate Bare Board electrical test requirements, when applicable:

Note: Refer to note #23 under ''Example of typical notes.''

☐ Master Drawing Revision Control: Master Drawing Revision Level and Bare Board Revision Level: Refer to 3.10 and select one of the three options illustrated:
Option I (preferred method), 3.10.1
Option II (permissible method), 3.10.2
Option III (permissible method), 3.10.3

☐ Configuration Control (3.20 and 4.3.6)
Prepare an Artwork Configuration Control chart, Figure 3-1, 3-2, and 3-3, illustrating Artwork Layers, Drawing Number, Revision Levels, Copper Weight, and Nominal Finished Conductor (line) Width.

☐ Board Construction/Cross Sectional View (4.2.5)
Prepare a cross-sectional view or exploded view illustrating the construction and lay-up of the board (Figures 4-4 and 4-4A). Indicate impedance values (for each layer) and dielectric value used to calculate impedance values. A special test coupon may be added and used for impedance measurements. When the fabricator is required to measure impedance values, a special note **shall** be added indicating the requirements.

☐ Hole Schedule (4.3.7, Figures 4-7 and 4-8) Delineate all hole diameters and tolerances; assign a code letter and drill letter for every unique drilled hole diameter and identify those holes which are plated, non-plated and tented. When using liquid photoimageable (LPI) solder mask and one side is partially plugged, add a small auxiliary view to illustrate the side being plugged. Identify tooling holes, since most tooling holes must be held to much tighter tolerances.

☐ Marking and Legends (4.3.1 and 4.3.2) Indicate marking requirements and their locations. Be sure to include

marking ink requirements (or other marking requirements), date code requirements and locations, fabricator's I.D. and U.L. marking requirements and location.

☐ Quality Conformance Coupons (Figure 4-10) Indicate locations of coupons and include all coupon marking requirements.

☐ Drill Pattern (Figure 4-8) Prepare a drill pattern, part of the Master Drawing requirements. This is a separate view used to identify all hole locations and diameters. The drill pattern may be a pen plot, photo plot or photographic composite copy produced at a 1:1 scale where symbols are used to represent each unique hole diameter.

☐ Profile (Board Outline) (4.3.9, Figures 4-9 and 4-9a) Prepare a profile view, part of the Master Drawing requirements. This is a separate view, depicting all necessary dimensions. The dimensioning and tolerancing conventions **shall** be in accordance with IPC-D-300.

☐ Master Pattern Drawing (4.2.3 and Figure 4-1) is part of the Master Drawing set and may be supplied using one of the following two options:

Option #1: Reproduction of original artwork or database supplied on drawing formats.

Option #2: Electronic data, in lieu of reproductions, as noted above.

☐ Review for completion of all drawing requirements, refer to 3.3 through 3.21. Included are the following: Title block, titles and subtitles, sign-off column, multiple sheet numbering and revision status of sheets (Figures 3-4, 3-5, and 3-6). Preliminary release and/or initial release, refer to Table 3-1; Revision letters, contract number and application block, refer to 3.12 through 3.16.

Commercial and Government Entity (Cage Code), Distribution Key and Material Block Location (Figure 3-4 and 3.17 through 3.19).

7.0 DESIGN OUTPUTS

Outputs of the detailed design are the final technical documents used for purchasing, fabrication, assembly, de-bug and test, inspection, installation and field service.

Includes:

- Drawings & Parts Lists
- Specifications
- Instructions
- Data

7.1 Design Verification Includes the following five design control measures:

- Design Reviews
- Qualification Tests
- Alternative Calculations
- Comparison with Proven Designs
- Drawing Check and Review

7.2 Final Documentation Package The final documentation package **shall** include, but not be limited to the following:

The preferred method for generation of CAD data output is IPC-D-35X series format. Refer to IPC-D-350; this standard specifies record formats used to describe printed board products with detail sufficient for tooling, manufacturing, and testing requirements. These records are also useful when the manufacturing cycle includes computer aided processes and numerically controlled machines. Refer to Tables 4-1 and 4-2.

7.3 CAD System Outputs IPC-D-35X Series format is the preferred output format (see 7.2). The CAD system outputs illustrated below have been in use for many years and are still very popular. The following outputs are shown for illustration purposes only. CAD system outputs may include but are not limited to the following:

CAD system outputs:

- Aperture List (Ascii format)
- Special A/W Features (HPGL format)
- Artwork Layers (Gerber format)
- Solder Mask(s) (Gerber format)
- Silkscreen(s) (Gerber format)
- Solder Paste Screen(s) (Gerber format)
- N.C. Drill Data & Drill Bit List (Excellon format)
- N.C. Board Profile Routing Data (N.C. data)
- Electrical Test Data (Bare Board)(IPC-D-356 format)
- Netlist (Ascii format)
- Automatic Component Insertion Data
- Surface Mount Pick and Place Data
- Assembly Drawing and Parts List (HPGL format)
- Functional Test Data (ATE) (Assembled Board) (GenRad format)
- Schematic/Logic Diagram (HPGL format)

7.4 Data Transfer Data may be transferred electronically across a local area network (LAN) and/or by modem. Other means of data transfer includes use of magnetic media; i.e., floppy diskettes or magnetic tape. All data files or magnetic media **shall** be identified with header information or labels containing the following information:

- Company Name (ownership)
- Board Number, Revision and Date
- Format (IPC, Gerber, Excellon, etc.)
- File Name (Layer and Number)

7.5 Readme File When transferring data electronically, it is suggested that designers include a readme.txt file, prepared in Ascii format and transmitted along with the design data (Figure 7-1).

8.0 PRINTED BOARD ASSEMBLY DRAWINGS

Information contained in this section outlines requirements to be considered when preparing the Printed Board Assembly Drawing and related parts list. The following examples