– Maximum continuous voltage:
  - at least 1,25 times the **rated voltage** of the equipment; or
  - at least 1,25 times the upper voltage of the **rated voltage range**.

  NOTE The maximum continuous voltages are not limited to values specified in 2.1.2 of IEC 61051-2:1991 or the values in Table 1 and Table 2 of IEC 61643-331:2017, other voltages can be used.

– Combination pulse (Table I group 1 of IEC 61051-2:1991/AMD1:2009 or 8.1.1 of IEC 61643-331:2017, Figure 4).

  For the test, a combination pulse is selected from 2.3.6 in IEC 61051-2:1991/AMD1:2009 or from 8.1.1 of IEC 61643-331:2017, Figure 4. The test consists of 10 positive pulses or 10 negative pulses, each having a shape of 1,2/50 μs for voltage and 8/20 μs for current.

  For the selection, AC **mains** voltage and overvoltage category, see Table 12.

  Mains under 300 V is considered to be 300 V.

  For Overvoltage Category IV of Table 12, a combination pulse 6kV/3kA is used except for 600 V, for which a combination pulse of 8 kV/4 kA is used. As an alternative, the combination pulse test of IEC 61051-2:1991/AMD1:2009 (2.3.6, Table I group 1 and Annex A) or the combination pulse test of 8.1.1 Figure 4 of IEC 61643-331:2017, including consideration of the nominal **mains** voltage and overvoltage category, is acceptable.

  After the test, the varistor voltage at the manufacturer's specified current shall not have changed by more than 10 % when compared to the value before the test.

The body of surge suppression varistor shall comply with the needle flame according to IEC 60695-11-5, with the following test severities:

– Duration of application of the test flame: 10 s.
– After flame time: 5 s.

If the body of surge suppression varistor complies with **V-1 class material**, the needle flame test does not need to be performed.

NOTE 1 A varistor is sometimes referred to as an MOV or a VDR.

NOTE 2 Nominal varistor voltage is a voltage, at a specified DC current, used as a reference point in the component characteristic (see IEC 61051-1).

G.8.2 Safeguards against fire

G.8.2.1 General

This subclause applies to varistors used as a **safeguard** against fire:

– when the method “reduce the likelihood of ignition” of 6.4.1 is chosen; or
– when the method “control fire spread” of 6.4.1 is chosen and the **enclosure** is made of **combustible material** and located less than 13 mm from the varistor.

The **safeguards** in this subclause are not applicable to a varistor used in a suppression circuit whose nominal varistor voltage, as specified in IEC 61051-1, is above AC **mains transient voltage**.

A varistor shall be regarded as a **PIS**.

The varistor overload test of G.8.2.2 and the **temporary overvoltage** test of G.8.2.3 shall be performed depending on the maximum continuous AC voltage of the varistor according to Table G.10.

Table G.10 – Varistor overload and temporary overvoltage test

Maximum continuous AC voltage of a varistor	Connection between		
	L to N or L to L	L to PE	N to PE
1,25 × V_r to 2 × V_r	G.8.2.2	G.8.2.2 and G.8.2.3	G.8.2.2 and G.8.2.3
Over 2 × V_r to 1 200 + 1,1 × V_r	No test	G.8.2.3	G.8.2.3
Over 1 200 + 1,1 × V_r	No test	No test	No test
V_r is the **rated voltage** or the upper voltage of the **rated voltage range** of the equipment.			

G.8.2.2 Varistor overload test

*The following test is simulated as required by Table G.10 to either a varistor or a surge suppression circuit containing varistors connected across the **mains** (L to L or L to N), line to protective earth (L to PE), or neutral to protective earth (N to PE).*

The following test simulation circuit shall be used:

- *Voltage is the AC source of 2 × V_r.*
- *Current is the current resulted from a test resistor R_x connected in series with the AC source.*
- *V_r is the **rated voltage** or the upper voltage of the **rated voltage range** of the equipment.*

The test shall be performed with an initial test resistor R_1 = 16 × V_r.

If the circuit does not open immediately during the initial application of test current, the test shall be continued until temperature stability (see B.1.5).

Subsequently, the test shall be repeated with new values of R_x (R_2, R_3, R_4, etc.) until the circuit opens, where:

- R_2 = 8 × V_r Ω
- R_3 = 4 × V_r Ω
- R_4 = 2 × V_r Ω
- R_x = 0,5 × (R_{x-1}) × V_r Ω.

Components in parallel with the varistor that may be affected by this test shall be disconnected.

*During and following the test, there shall be no risk of fire and **equipment safeguards**, other than the varistor under test, shall remain effective.*

During the test, the circuit may:

- *open due to the operation of a protective device such as a fuse, a thermal fuse; or*
- *close due to the operation of a GDT.*

G.8.2.3 Temporary overvoltage test

*The **temporary overvoltage** test is simulated by the following test methods where applicable:*

*A surge suppression circuit containing varistors connected between the **mains** conductors and the earth is tested according to 8.3.8.1 and 8.3.8.2 of IEC 61643-11:2011. The*

compliance criteria of B.4.8 may be used as an alternative to the compliance criteria of IEC 61643-11.

If a surge suppression circuit is used, the combination pulse specified in G.8.2 is applied before this test.

During the test, the circuit may:

– *open due to the operation of a protective device such as a thermal fuse; or*

– *close due to the operation of a GDT.*

NOTE For different power distribution systems, the **temporary overvoltages** are defined in Annex B of IEC 61643-11:2011.

Components in parallel with the varistor that may be affected by this test shall be disconnected.

G.9 Integrated circuit (IC) current limiters

G.9.1 Requirements

IC current limiters used for current limiting in power sources so that the available output power becomes PS1 or PS2 are not shorted from input to output if they comply with all of the following:

– the IC current limiters limit the current to manufacturer's defined value (not to be more than 5 A) under **normal operating conditions** with any specified drift taken into account;

– the IC current limiters are entirely electronic and have no means of manual operation or reset;

– the IC current limiters output current is limited to 5 A or less (specified maximum load);

– the IC current limiters limit the current or voltage to the required value with the manufacturer's defined drift, as applicable, taken into account after each of the conditioning tests; and

– the test program as specified in G.9.2.

G.9.2 Test program

The test program consists of the performance tests outlined in Table G.11*.*

The following specifications are to be supplied by the manufacturer for application of tests:

– *power source limitation/specification (if less than 250 VA);*

– *maximum input voltage (volts); and*

– *maximum output load (amperes).*

Six samples are used for testing as follows:

Sample 1: Line 1

Sample 2: Lines 2 and 3

Sample 3: Lines 4 and 5

Sample 4: Line 6

Sample 5: Line 7

Sample 6: Line 8.

The power source for the tests should be capable of delivering 250 VA minimum, unless the IC current limiter has a lower specification or is tested in the end product.

Table G.11 – Performance test program for integrated circuit (IC) current limiters

Line	Test category	Test condition	Cycles	Device condition temperature °C [a b c]	Device enable voltage	Device input voltage	Device output load (amperes) to RTN [d,e]
1	Start up	Enable pin – cycle	10 000	25	Off to On	Maximum (rated)	Maximum (rated)
2	"	Enable pin – cycle	50	70	Off to On	Maximum (rated)	0 Ω || 470 µF
3	"	Enable pin – cycle	50	-30	Off to On	Maximum (rated)	0 Ω || 470 µF
4	"	Input power pin – cycle	50	70	On	Maximum (rated)	0 Ω || 470 µF
5	"	Input power pin – cycle	50	-30	On	Maximum (rated)	0 Ω || 470 µF
6	Short Circuit	Output power pin – short circuit	50	70	On	Maximum (rated)	Open to 0 Ω (open to short)
7	Overload	Enable pin – cycle	50	25	Off to On	Maximum (rated)	150 % maximum
8	"	Input power pin – cycle	50	25	On	Maximum (rated)	150 % maximum

RTN = Return

\|\| = in parallel

[a] T_{ma} not applied

[b] ± 2 °C

[c] sample conditioned 3 h before test

[d] ± 20 %

[e] Load should be implemented through a suitably rated capacitor and a parallel conductive wire providing similar characteristics to a shorted, zero ohm (0 Ω) resistive load. The capacitor voltage rating should be not less than the maximum voltage rating of the component under test.

G.9.3 Compliance criteria

After the test program, the device shall limit the current in accordance with its specification as applicable or the device shall become open circuit. The open circuited device is replaced with a new sample and tests continued as applicable.

G.10 Resistors

G.10.1 General

For each of the tests in this clause, ten samples of resistors are tested. A sample is a single resistor if used alone or a group of resistors as used in the application. Prior to each test, the resistance of the samples is measured, followed by the conditioning of G.10.2.

G.10.2 Conditioning

The samples shall be subjected to the damp heat test according to IEC 60068-2-78, with the following details:

– *temperature:* *(40 ± 2) °C;*

– *humidity:* *(93 ± 3) % relative humidity;*

– *test duration:* *21 days.*

G.10.3 Resistor test

Each sample is then subjected to 10 impulses of alternating polarity, using the impulse test generator circuit 2 of Table D.1. The interval between successive impulses is 60 s, and U_C is equal to the applicable ***required withstand voltage****.*

After the test, the resistance of each sample shall not have changed by more than 10 %. No failure is allowed.

The lowest resistance value of the ten samples tested is used to measure the current when determining compliance with Table 4*.*

G.10.4 Voltage surge test

Each sample is subjected to 50 discharges from the impulse test generator circuit 3 of Table D.1, at not more than 12 discharges per minute, with U_C equal to 10 kV.

After the tests, the resistance of each sample shall not have changed by more than 20 %. No failure is allowed.

G.10.5 Impulse test

Each sample is subjected to 10 pulses from the impulse test generator circuit 1 of Table D.1, with U_C equal to 4 kV or 5 kV of alternating polarity with a minimum of 60 s interval between pulses as applicable (see Table 13).

After the tests, the resistance of each sample shall not have changed by more than 20 %. No failure is allowed.

G.10.6 Overload test

The samples are each subjected to a voltage of such a value that the current through it is 1,5 times the value measured through a resistor, having a resistance equal to the specified rated value, which is fitted to the equipment, when operated under ***single fault conditions****. During the test the voltage is kept constant. The test is performed until thermal steady state is reached.*

After the tests, the resistance of each sample shall not have changed by more than 20 %. No failure is allowed.

G.11 Capacitors and RC units

G.11.1 General

The requirements below specify conditioning criteria when testing capacitors and RC units or discrete components forming an RC unit and serving as **safeguards** and provides selection criteria for capacitors and RC units that comply with IEC 60384-14.

G.11.2 Conditioning of capacitors and RC units

When required by 5.5.2.1, the following conditioning is applied when evaluating a capacitor or an RC unit to the requirements of IEC 60384-14.

The duration of the damp heat, steady state test as specified in 4.12 of IEC 60384-14:2005, shall be 21 days at a temperature of (40 ± 2) °C and a relative humidity of (93 ± 3) %.

Capacitors subjected to a duration that is longer than 21 days during the above test are considered acceptable.

G.11.3 Rules for selecting capacitors

The appropriate capacitor subclass shall be selected from those listed in Table G.12, according to the rules of application in the table.

Table G.12 – Capacitor ratings according to IEC 60384-14

Capacitor subclass according to IEC 60384-14	Rated voltage of the capacitor V RMS	Type test impulse test voltage of the capacitor kV peak	Type test RMS test voltage of the capacitor kV RMS
Y1	Up to and including 500	8	4
Y2	Over 150 up to and including 300	5 [a]	1,5
Y4	Up to and including 150	2,5	0,9
X1	Up to and including 760	4 [a]	-
X2	Up to and including 760	2,5 [a]	-

Rules for the application of this table.

1 The voltage rating of the capacitor shall be at least equal to the **RMS working voltage** across the insulation being bridged, determined according to 5.4.1.8.2. As an exception to the requirements in the table, one Y2 capacitor may be used in cases where 2,5 kV is required.

2 For a single capacitor (X type) serving as **functional insulation**, failure of the capacitor shall not result in the failure of a **safeguard** and the **type test** impulse test voltage shall be at least equal to the **required withstand voltage**.

3 A higher grade capacitor than the one specified may be used, as follows:

- subclass Y1 if subclass Y2 is specified;
- subclass Y1 or Y2 if subclass Y4 is specified;
- subclass Y1 or Y2 if subclass X1 is specified;
- subclass X1, Y1 or Y2 if subclass X2 is specified.

4 Two or more capacitors may be used in series in place of the single capacitor specified, as follows:

- subclass Y1 or Y2 if subclass Y1 is specified;
- subclass Y2 or Y4 if subclass Y2 is specified;
- subclass X1 or X2 if subclass X1 is specified.

5 If two or more capacitors are used in series they shall comply with 5.5.2.1 as applicable and comply with the other rules above.

[a] For capacitance values of more than 1 μF, this test voltage is reduced by a factor equal to $\sqrt{C}$, where C is the capacitance value in μF.

G.12 Optocouplers

Optocouplers shall comply with the requirements of IEC 60747-5-5:2007. In the application of IEC 60747-5-5:2007,

– the **type testing** as specified in 7.4.3 of IEC 60747-5-5:2007 shall be performed with a voltage $V_{ini,a}$ that is at least equal to the appropriate test voltage in 5.4.9.1 of this document; and

– the **routine testing** as specified in 7.4.1 of IEC 60747-5-5:2007 shall be performed with a voltage $V_{ini,b}$ that is at least equal to the appropriate test voltage in 5.4.9.2 of this document.

G.13 Printed boards

G.13.1 General

The requirements for **basic insulation**, **supplementary insulation**, **reinforced insulation** and **double insulation** on printed boards are specified below.

These requirements also apply to the windings of a planar transformer.

G.13.2 Uncoated printed boards

The insulation between conductors on the outer surfaces of an uncoated printed board shall comply with the minimum **clearance** requirements of 5.4.2 and the minimum **creepage distance** requirements of 5.4.3.

Compliance is checked by inspection and by measurement.

G.13.3 Coated printed boards

The requirements for separation distances before the boards are coated are specified below.

An alternative method to qualify coated printed boards is given in IEC 60664-3.

For printed boards whose outer surfaces are to be coated with a suitable coating material, the minimum separation distances of Table G.13 apply to conductive parts before they are coated.

Double insulation and **reinforced insulation** shall pass **routine tests** for electric strength of 5.4.9.2.

Either one or both conductive parts and the entire distances over the surface between the conductive parts shall be coated.

The minimum **clearances** of 5.4.2 and the minimum **creepage distances** of 5.4.3 shall apply:

– if the above conditions are not met;
– between any two uncoated conductive parts; and
– over the outside of the coating.

Compliance is checked by inspection and measurement, taking Figure O.11 and Figure O.12 into account, and by the tests of G.13.6.

Table G.13 – Minimum separation distances for coated printed boards

Peak of the working voltage up to and including V peak	Basic insulation or supplementary insulation mm	Reinforced insulation mm
71 [a]	0,025	0,05
89 [a]	0,04	0,08
113 [a]	0,063	0,125
141 [a]	0,1	0,2
177 [a]	0,16	0,32
227 [a]	0,25	0,5
283 [a]	0,4	0,8
354 [a]	0,56	1,12
455 [a]	0,75	1,5
570	1,0	2,0
710	1,3	2,6
895	1,8	3,6
1 135	2,4	3,8
1 450	2,8	4,0
1 770	3,4	4,2
2 260	4,1	4,6
2 830	5,0	5,0
3 540	6,3	6,3
4 520	8,2	8,2
5 660	10	10
7 070	13	13
8 910	16	16
11 310	20	20
14 140	26	26
17 700	33	33
22 600	43	43
28 300	55	55
35 400	70	70
45 200	86	86
Linear interpolation may be used between the nearest two points, the calculated spacing being rounded up to the next higher 0,1 mm increment.		
[a] The test of G.13.6 is not required.		

G.13.4 Insulation between conductors on the same inner surface

The requirements for insulation on the same inner layer of a multilayer board are specified below.

On an inner surface of a multi-layer printed board (see Figure O.14), the path between any two conductors shall comply with the requirements for a cemented joint in 5.4.4.5.

G.13.5 Insulation between conductors on different surfaces

The requirements for insulation on the different layers of a multilayer board are specified below.

For **basic insulation** there is no thickness requirement.

Supplementary insulation or **reinforced insulation** between conductive parts on different surfaces in double-sided single-layer printed boards, multi-layer printed boards and metal core printed boards, shall either have a minimum thickness of 0,4 mm provided by a single layer or conform with one of the specifications and pass the relevant tests in Table G.14.

Table G.14 – Insulation in printed boards

Specification of insulation	Type tests [a]	Routine tests for electric strength [c]
Two layers of sheet insulating material including pre-preg [b]	No	Yes
Three or more layers of sheet insulating material including pre-preg [b]	No	No
An insulation system with ceramic coating over a metallic substrate, cured at ≥ 500 °C	No	Yes
An insulation system, with two or more coatings other than ceramic over a metallic substrate, cured at < 500 °C	Yes	Yes
NOTE 1 Pre-preg is the term used for a layer of glass cloth impregnated with a partially cured resin. NOTE 2 For definition of ceramic, see IEC 60050-212:2010, 212-15-25.		
[a] Thermal conditioning of G.13.6.2 followed by the electric strength test of 5.4.9.1. [b] Layers are counted before curing. [c] Electric strength testing is carried out on the finished printed board.		

G.13.6 Tests on coated printed boards

G.13.6.1 Sample preparation and preliminary inspection

Three sample printed boards (or, for coated components in Clause G.14, two components and one board) identified as samples 1, 2 and 3 are required. Either actual boards or specially produced samples with representative coating and minimum separations may be used. Each sample board shall be representative of the minimum separations used, and coated. Each sample is subjected to the full sequence of manufacturing processes, including soldering and cleaning, to which it is normally subjected during equipment assembly.

When visually inspected, the boards shall show no evidence of pinholes or bubbles in the coating or breakthrough of conductive tracks at corners.

G.13.6.2 Test method and compliance criteria

Sample 1 is subjected to the thermal cycling sequence of 5.4.1.5.3.

Sample 2 is aged in a full draught oven at a temperature and for a time duration chosen from the graph shown in Figure G.3 using the temperature index line that corresponds to the maximum operating temperature of the coated board. The temperature of the oven is maintained at the specified temperature ± 2 °C. The temperature used to determine the temperature index line is the highest temperature on the board where safety is involved.

When using Figure G.3, interpolation may be used between the nearest two temperature index lines.

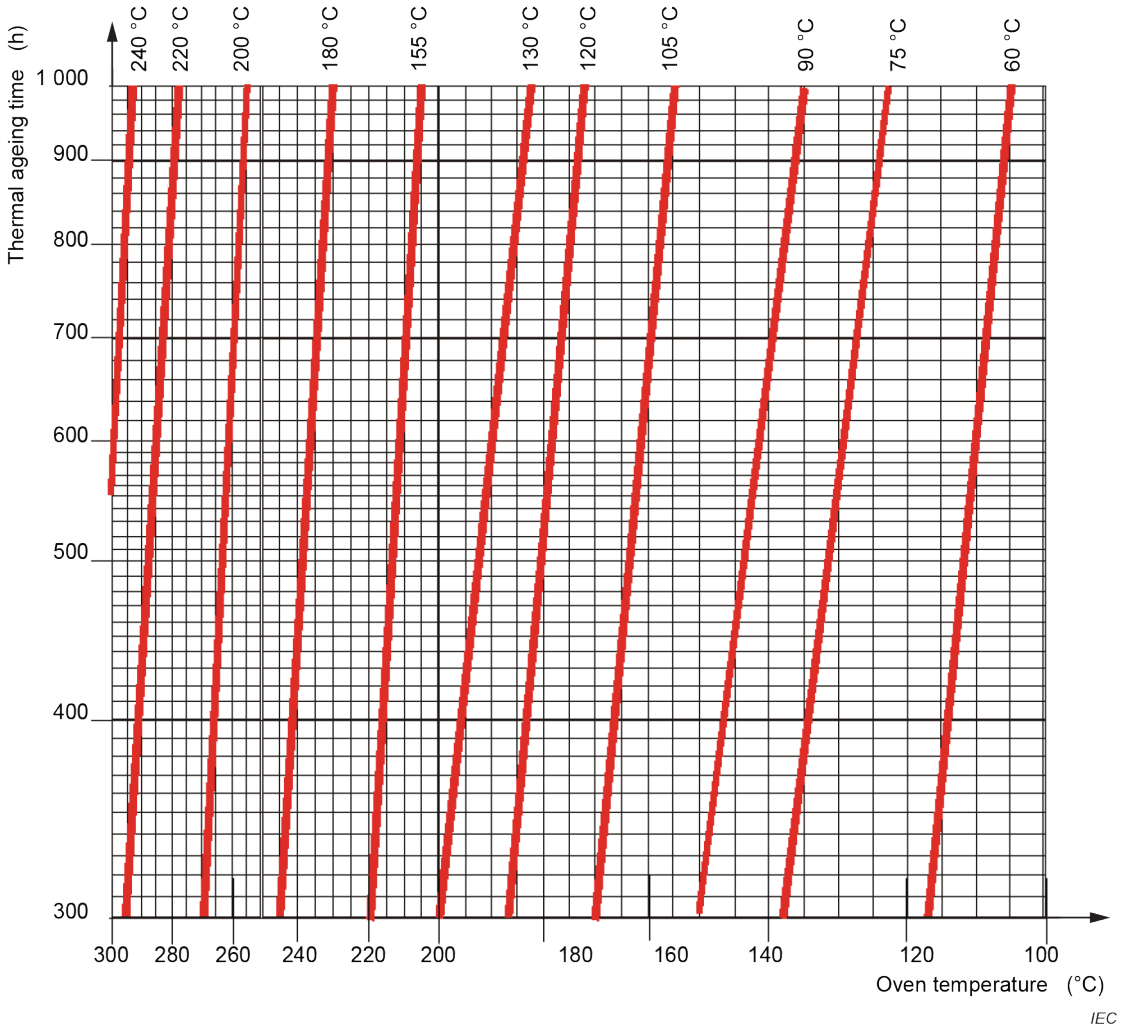


Figure G.3 – Thermal ageing time

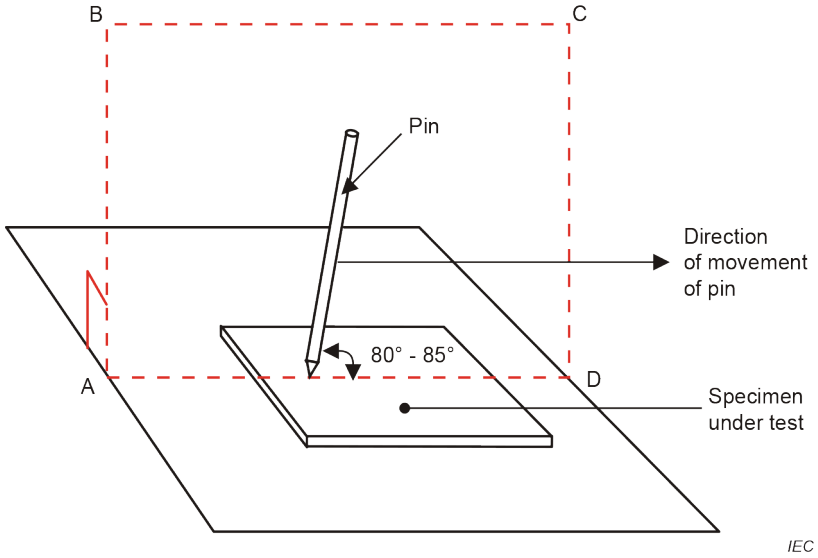
Samples 1 and 2 are then subjected to the humidity conditioning of 5.4.8 and shall withstand the electric strength test of 5.4.9.1 between conductors.

Sample board 3 is subjected to the following abrasion resistance test:

Scratches are made across five pairs of conducting parts and the intervening separations at points where the separations will be subject to the maximum potential gradient during the tests.

The scratches are made by means of a hardened steel pin, the end of which has the form of a cone having a tip angle of 40°, its tip being rounded and polished, with a radius of 0,25 mm ± 0,02 mm.

Scratches are made by drawing the pin along the surface in a plane perpendicular to the conductor edges at a speed of 20 mm/s ± 5 mm/s as shown in Figure G.4. The pin is so loaded that the force exerted along its axis is 10 N ± 0,5 N. The scratches shall be at least 5 mm apart and at least 5 mm from the edge of the specimen.



NOTE The pin is in the plane ABCD that is perpendicular to the specimen under test.

Figure G.4 – Abrasion resistance test for coating layers

After the test, the coating layer shall neither have loosened nor have been pierced. The coating shall withstand an electric strength test as specified in 5.4.9.1 between conductors. In the case of metal core printed boards, the substrate is one of the conductors.

If mechanical stress or bending is applied to the board, additional tests to identify cracking may be needed (see IEC 60664-3).

G.14 Coatings on component terminals

G.14.1 Requirements

The requirements for coatings on component terminals and the like, where the coating is used to reduce **clearances** and **creepage distances** are specified below.

Coatings may be used over external terminations of components to increase effective **clearances** and **creepage distances** (see Figure O.11). The minimum separation distances of Table G.13 apply to the component before coating, and the coating shall meet all the requirements of G.13.3. The mechanical arrangement and rigidity of the terminations shall be adequate to ensure that, during normal handling, assembly into equipment and subsequent use, the terminations will not be subject to deformation that would crack the coating or reduce the separation distances between conductive parts below the values in Table G.13 (see G.13.3).

G.14.2 Test method and compliance criteria

Compliance is checked by inspection taking into account Figure O.11 and by applying the sequence of tests covered by G.13.6. These tests are carried out on a completed assembly including the component(s).

The abrasion resistance test of G.13.6.2 is carried out on a specially prepared sample printed board as described for sample 3 in G.13.6.1, except that the separation between the conductive parts shall be representative of the minimum separations and maximum potential gradients used in the assembly.