– First reference voltage $u_1 = 0{,}75 \times k_{pp} \times U_r \sqrt{\frac{2}{3}}$

– Time t_1 for terminal fault test-duties is derived from u_1 and the specified value of the rate of rise u_1/t_1. For test-duties OP1 and OP2, t_1 is two times t_1 for test-duty T100 and the rate of rise is derived from u_1 and t_1. For the supply side circuit of short-line fault, time t_1 is derived from u_1 and the specified value of the rate of rise u_1/t_1 which is the same as for test-duty T100.

– TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \times \sqrt{\frac{2}{3}}$

where k_{af} is equal to 1,4 for test-duty T100 and for the supply side circuit for SLF, 1,5 for test-duty T60, 1,54 for test-duty T30, 1,76 for test-duty T10 in case of k_{pp} is 1,3, 1,53 (0,9 × 1,7) for test-duty T10 in the case of k_{pp} is 1,5, and 1,25 for out-of-phase breaking.

– Time t_2 is equal to $4t_1$ for test-duty T100 and for the supply side circuit for short-line fault and between t_2 (for T100) and $2t_2$ (for T100) for out-of-phase breaking. Time t_2 is equal to $6t_1$ for T60.

– For test-duties T30 and T10, time t_3 is derived from u_c and the specified value of the rate of rise u_c/t_3.

– Time delay t_d is 2 μs for test-duty T100, between 2 μs and $0{,}3t_1$ for test-duty T60, between 2 μs and $0{,}1t_1$ for test-duties OP1 and OP2. Time delay is 0,15 t_3 for test-duties T30 and T10. For the supply side circuit for short-line fault the time delay is equal to 2 μs. When short-line fault tests are performed, the time delay t_d for test-duty T100 can be extended up to 0,28 t_1. The relevant value of t_d to be used for testing is given in 7.105.5.2 to 7.105.5.5.

– Voltage u' = $u_1/2$ for test-duties T100 and T60 and the supply side for SLF and out-of-phase breaking, and $u_c/3$ for test-duties T30 and T10.

– Time t' is derived from u', u_1/t_1 and t_d for test-duties T100, T60 and the supply circuit for SLF and out-of-phase breaking, and according to Figure 42; and from u', u_c/t_3 and t_d for test-duties T30 and T10 according to Figure 43.

c) *For rated voltages higher than 800 kV*

A representation by four parameters of the prospective TRV is used for test-duties T100 and T60, and the supply circuit of SLF for test-duties L_{90} and L_{75} and by two parameters for test-duties T30, T10 and for out-of-phase test-duties OP1 and OP2.

– First reference voltage $u_1 = 0{,}75 \times k_{pp} \times U_r \sqrt{\frac{2}{3}}$

– Time t_1 for terminal fault test-duties is derived from u_1 and the specified value of the rate of rise u_1/t_1. For the supply side circuit of short-line fault, time t_1 is derived from u_1 and the specified value of the rate of rise u_1/t_1 which is the same as for test-duty T100.

– Time t_3 for out-of-phase test-duties OP1 and OP2 is derived from u_c and the specified value of the rate of rise.

– TRV peak value $u_c = k_{pp} \times k_{af} \times U_r \sqrt{\frac{2}{3}}$

where k_{af} is equal to 1,5 for test-duty T100 and for the supply side circuit for SLF, 1,5 for test-duty T60, 1,54 for test-duty T30, 1,76 for test-duty T10, and 1,25 for out-of-phase breaking.

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- Time t_2 is equal to 3 t_1 for test-duty T100 and for the supply side circuit for short-line fault. Time t_2 is equal to 4,5 t_1 for T60.
- For test-duties T30 and T10, time t_3 is derived from u_c and the specified value of the rate of rise u_c/t_3.
- Time delay t_d is 2 μs for test-duty T100, between 2 μs and 0,3 t_1 for test-duty T60. Time delay is 0,15 t_3 for test-duties T30 and T10, 0,05 t_3 for test-duties OP1 and OP2. For the supply side circuit for short-line fault the time delay is equal to 2 μs. When short-line fault tests are performed, the time delay t_d for test-duty T100 can be extended up to 0,28 t_1. The relevant value of t_d to be used for testing is given in 7.105.5.2 to 7.105.5.5.
- Voltage u' = $u_1/2$ for test-duties T100 and T60 and the supply side for SLF, and $u_c/3$ for test-duties T30, T10 and out-of-phase test-duties.
- Time t' is derived from u', u_1/t_1 and t_d for test-duties T100, T60 and the supply circuit for SLF, and according to Figure 42; and from u', u_c/t_3 and t_d for test-duties T30, T10 and out-of-phase test-duties according to Figure 43.

For rated voltages of 100 kV and above, the specified values are given in Table 20 and Table 21.

Table 20 – Values of prospective TRV for circuit-breakers rated for k_{pp} = 1,2 or 1,3 – Rated voltages of 100 kV and above

U_r	Test-duty	k_{pp}	k_{af}	u_1	t_1	u_c	t_2 or t_3	t_d [a]	u'	t' [a]	u_1/t_1 u_c/t_3
kV		p.u.	p.u.	kV	μs	kV	μs	μs	kV	μs	kV/μs
100	T100	1,3	1,40	80	40	149	160	2 (11)	40	22 (31)	2
	T60	1,3	1,50	80	27	159	162	2-8	40	15-21	3
	T30	1,3	1,54	-	-	163	33	5	54	16	5
	T10	1,3	1,76	-	-	187	27	4	62	13	7
123	T100	1,3	1,40	98	49	183	196	2 (14)	49	26 (38)	2
	T60	1,3	1,50	98	33	196	198	2-10	49	18-26	3
	T30	1,3	1,54	-	-	201	40	6	67	19	5
	T10	1,3	1,76	-	-	230	33	5	77	16	7
145	T100	1,3	1,40	115	58	215	232	2 (16)	58	31 (45)	2
	T60	1,3	1,50	115	38	231	228	2-12	58	21-31	3
	T30	1,3	1,54	-	-	237	47	7	79	23	5
	T10	1,3	1,76	-	-	272	39	6	91	19	7
170	T100	1,3	1,40	135	68	253	272	2 (19)	68	36 (53)	2
	T60	1,3	1,50	135	45	271	270	2-14	68	25-36	3
	T30	1,3	1,54	-	-	278	56	8	93	27	5
	T10	1,3	1,76	-	-	319	46	7	106	22	7
245	T100	1,3	1,40	195	98	364	392	2 (27)	98	51 (76)	2
	T60	1,3	1,50	195	65	390	390	2-20	98	35-52	3
	T30	1,3	1,54	-	-	400	80	12	133	39	5
	T10	1,3	1,76	-	-	459	66	10	153	32	7

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U_r	Test-duty	k_{pp}	k_{af}	u_1	t_1	u_c	t_2 or t_3	t_d [a]	u'	t' [a]	u_1/t_1 u_c/t_3
300	T100	1,3	1,40	239	119	446	476	2 (33)	119	62 (93)	2
	T60	1,3	1,50	239	80	478	480	2-24	119	42-64	3
	T30	1,3	1,54	-	-	490	98	15	163	47	5
	T10	1,3	1,76	-	-	562	80	12	187	39	7
362	T100	1,3	1,40	288	144	538	576	2 (40)	144	74 (112)	2
	T60	1,3	1,50	288	96	576	576	2-29	144	50-77	3
	T30	1,3	1,54	-	-	592	118	18	197	57	5
	T10	1,3	1,76	-	-	678	97	15	226	47	7
420	T100	1,3	1,40	334	167	624	668	2 (47)	167	86 (130)	2
	T60	1,3	1,50	334	111	669	666	2-33	167	58-89	3
	T30	1,3	1,54	-	-	687	137	21	229	66	5
	T10	1,3	1,76	-	-	787	112	17	262	54	7
550	T100	1,3	1,40	438	219	817	876	2 (61)	219	111 (171)	2
	T60	1,3	1,50	438	146	876	876	2-44	219	75-117	3
	T30	1,3	1,54	-	-	899	180	27	300	87	5
	T10	1,3	1,76	-	-	1 031	147	22	344	71	7
800	T100	1,3	1,40	637	318	1 189	1 272	2 (89)	318	161 (248)	2
	T60	1,3	1,50	637	212	1 274	1 272	2-64	318	108-170	3
	T30	1,3	1,54	-	-	1 308	262	39	436	126	5
	T10	1,3	1,76	-	-	1 499	214	32	500	103	7
1 100	T100	1,2	1,50	808	404	1 617	1 212	2 (113)	404	204 (315)	2
	T60	1,2	1,50	808	269	1 617	1 212	2-81	404	137-216	3
	T30	1,2	1,54	-	-	1 660	332	50	553	161	5
	T10	1,2	1,76	-	-	1 897	271	41	632	131	7
1 200	T100	1,2	1,50	882	441	1 764	1 323	2 (123)	441	222 (343)	2
	T60	1,2	1,50	882	294	1 764	1 323	2-88	441	149-235	3
	T30	1,2	1,54	-	-	1 811	362	54	604	175	5
	T10	1,2	1,76	-	-	2 069	296	44	690	143	7

[a] Where two values of times t_d and t' are given for terminal fault test-duty T60, those indicate the lower and upper limits which should be used for testing. The time delay t_d and the time t' during testing should not be shorter than their respective lower limits and should not be longer than their respective upper limits.

Where two values of times t_d and t' are given for test-duty T100, separated by brackets, the time t_d in brackets is the upper limit of the time delay t_d that can be used for test-duty T100 if short-line fault tests are also made. For such cases, the delay line terminates at t' given in brackets. If this is not the case, the lower values of t_d and t' apply.

NOTE Test-duty T10 covers transformer-limited fault conditions with X_0/X_1 higher than 3,0 (for example non-effectively earthed transformers in effectively earthed neutral systems, or cases of transformers having one side effectively earthed and the other connected to non-effectively earthed neutral systems). For rated voltages higher than 170 kV the TRV specified covers also cases of 3-phase line faults with effectively earthed neutral systems where coupling between phases can lead to an amplitude factor of 1,76.

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Table 21 – Values of prospective TRV for circuit-breakers rated for k_{pp} = 1,5 – Rated voltages of 100 kV to 170 kV

U_r	Test-duty	k_{pp}	k_{af}	u_1	t_1	u_c	t_2 or t_3	t_d [a]	u'	t' [a]	u_1/t_1 u_c/t_3
kV		p.u.	p.u.	kV	µs	kV	µs	µs	kV	µs	kV/µs
100	T100	1,5	1,40	92	46	171	184	2 (13)	46	25 (36)	2
	T60	1,5	1,50	92	31	184	186	2-8	46	15-21	3
	T30	1,5	1,54	-	-	189	38	5	63	16	5
	T10	1,5	1,53	-	-	187	27	4	62	13	7
123	T100	1,5	1,40	113	56	211	224	2 (16)	56	30 (44)	2
	T60	1,5	1,50	113	38	226	228	2-10	56	18-26	3
	T30	1,5	1,54	-	-	232	46	6	77	19	5
	T10	1,5	1,53	-	-	230	33	5	77	16	7
145	T100	1,5	1,40	133	67	249	268	2 (19)	67	35 (52)	2
	T60	1,5	1,50	133	44	266	264	2-12	67	21-31	3
	T30	1,5	1,54	-	-	273	55	7	91	23	5
	T10	1,5	1,53	-	-	272	39	6	91	19	7
170	T100	1,5	1,40	156	78	291	312	2 (22)	78	41 (61)	2
	T60	1,5	1,50	156	52	312	312	2-14	78	25-36	3
	T30	1,5	1,54	-	-	321	64	8	107	27	5
	T10	1,5	1,53	-	-	319	46	7	106	22	7

[a] Where two values of times t_d and t' are given for terminal fault test-duty T60, those indicate the lower and upper limits which should be used for testing. The time delay t_d and the time t' during testing should not be shorter than their respective lower limits and should not be longer than their respective upper limits.

Where two values of times t_d and t' are given for test-duty T100, separated by brackets, the time t_d in brackets is the upper limit of the time delay t_d that can be used for test-duty T100 if short-line fault tests are also made. For such cases, the delay line terminates at t' given in brackets. If this is not the case, the lower values of t_d and t' apply.

NOTE Test-duty T10 covers transformer-limited fault conditions with X_0/X_1 higher than 3,0 (for example non-effectively earthed transformers in effectively earthed neutral systems, or cases of transformers having one side effectively earthed and the other connected to non-effectively earthed neutral systems).

The prospective TRV wave of the test circuit shall comply with the following two requirements:

– Requirement a)

Its envelope shall at no time be below the specified reference line.

It is stressed that the extent by which the envelope can exceed the specified reference line requires the consent of the manufacturer (see 7.105); this is of particular importance in the case of two-parameter envelopes when four-parameter reference lines are specified, and in the case of four-parameter envelopes when two-parameter reference lines are specified.

For convenience of testing it is allowed to carry out test-duties for which a four parameter TRV is specified with a two parameter TRV, provided that the rate-of-rise of recovery voltage corresponds to the standard value u_1/t_1 and the peak value to the standard value u_c. This procedure requires the consent of the manufacturer.

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– Requirement b)

Its initial portion shall fulfil the specified ITRV requirements. The ITRV shall be handled like a short-line fault. Consequently, it is necessary to measure the ITRV circuit independently of the source side in an inherent way. The ITRV is defined by the peak value u_i and the time coordinate t_i (Figure 45). The inherent waveshape shall mostly follow a straight line reference line drawn from the beginning of the ITRV to the point defined by u_i and t_i. The inherent ITRV waveshape shall follow this reference line from 20 % to 80 % of the required ITRV peak value. Deviations from the reference line are permitted for the ITRV amplitude below 20 % and above 80 % of the specified ITRV peak value. It shall not be significantly higher than the above-mentioned reference line. If the 80 % value cannot be reached without significant increase of the rate of rise of the ITRV, it is preferred to raise the peak value u_i above the specified value in order to reach the 80 % point. The rate of rise of the ITRV shall not be increased, because this would be connected to a change of the impedance and thus to an essential change of the severity of the test.

Testing under ITRV conditions is necessary for T100a, T100s and L_{90}. However, if a circuit-breaker with rated voltage equal or less than 800 kV has a short-line fault rating, the ITRV requirements are considered to be covered if L_{90} is carried out using a line with a time delay less than 100 ns (see also 7.105.5.2).

If a circuit-breaker with rated voltage higher than 800 kV has a short-line fault rating, the ITRV requirements are covered if L_{90} is carried out using a line with a time delay less than 100 ns and a surge impedance of 450 Ω (see also 7.105.5.2 and 7.109.3).

7.105.5.2 Test-duties T100s and T100a

For rated voltages less than 100 kV, the specified values are given in

– Table 16 and Table 17 for class S1 circuit-breakers,
– Table 18 and Table 19 for class S2 circuit-breakers.

The specific reference lines, delay lines and ITRV are given by the values in Table 9, Table 16, Table 17, Table 18, Table 19, Table 20 and Table 21.

With reference to ITRV, if a test is made with a TRV following the straight reference line specified in requirement a) and b) of 7.105.5.1 and shown in Figure 45, it is assumed that the effect on the circuit-breaker is similar to that of any ITRV defined in requirement b) of 7.105.5.1 and Figure 45.

Owing to limitations of the testing station, it may not be feasible to comply with the requirement of item b) of 7.105.5.1 with respect to the time delay t_d as specified in Table 16 through Table 21.

Where short-line fault duties are also to be performed, any such deficiency of the TRV of the supply circuit shall be compensated by an increase of the voltage excursion to the first peak of the line-side voltage (see 7.109.3). The time delay of the supply circuit shall be as small as possible, but shall in any case not exceed the values given in brackets in Table 18, Table 19, Table 20 or Table 21.

Where short-line fault duties are also to be performed, it may be convenient to combine the ITRV and L_{90} requirements in the line-side circuit. When the ITRV is combined with the transient voltage of a short line having a time delay t_{dL} as specified in 7.109.3 the total stress is, for practical considerations, equal or covered by the stress of a short line with a time delay less than 100 ns and a surge impedance of 450 Ω. Therefore the ITRV requirements for test-duties T100s and T100a are considered to be covered when L_{90} is performed using a line with a time delay less than 100 ns and a surge impedance of 450 Ω.

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Where short-line fault test-duty L_{90} with a time delay less than 100 ns is used to cover ITRV requirements, the initial part of the line side transient voltage up to 0,2 u_L* shall not cross the 20 % to 80 % L_{90} reference except if the time delay as defined in Figure 46 is less than 100 ns.

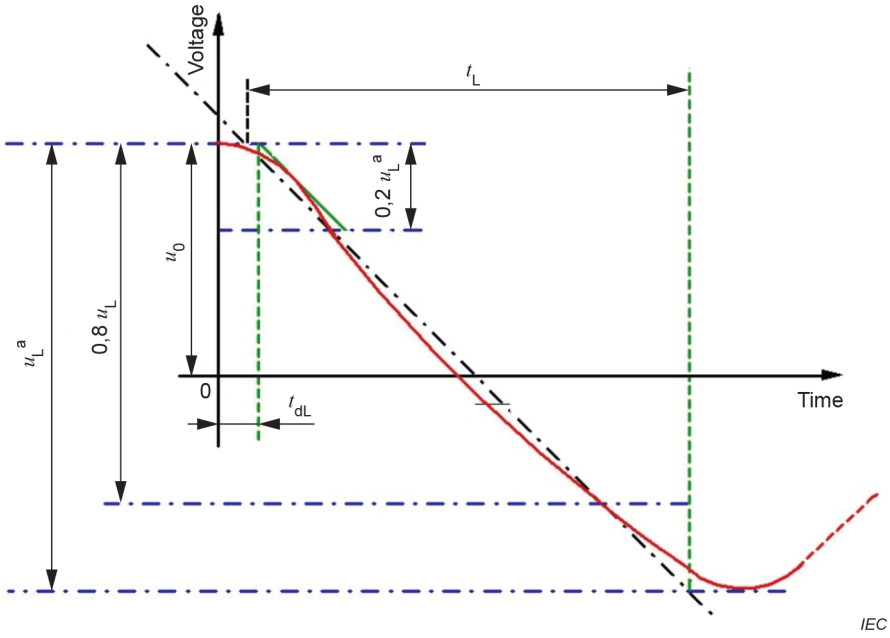

Figure 46 – Example of line transient voltage with time delay with non-linear rate of rise

7.105.5.3 Test-duty T60

For rated voltages less than 100 kV, the specified values are given in

– Table 16 and Table 17 for class S1 circuit-breakers,
– Table 18 and Table 19 for class S2 circuit-breakers.

For rated voltages of 100 kV and above, the specified standard values are given in Table 20 and Table 21.

7.105.5.4 Test-duty T30

a) For rated voltages less than 100 kV, the specified values are given in
   – Table 16 and Table 17 for class S1 circuit-breakers,
   – Table 18 and Table 19 for class S2 circuit-breakers.
b) For rated voltages of 100 kV and above, the specified standard values are given in Table 20 and Table 21.

In case that small values of time t_3 cannot be met, the shortest time that can be met shall be used. The values used shall be stated in the test report.

NOTE The contribution of transformers to the short-circuit current is relatively larger at smaller values of short-circuit current as in T30 and T10 conditions. However, most systems have effectively earthed neutrals at ratings of 100 kV up to 800 kV. With the system and transformer neutrals effectively earthed, a k_{pp} of 1,3 is applicable for all test-duties except for T10, where in general a k_{pp} of 1,5 is used in order to take also transformer fed faults into account. For rated voltages higher than 800 kV, a k_{pp} of 1,2 is applicable for all test-duties.

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In some systems for rated voltages of 100 kV up to and including 170 kV, transformers with non-effectively earthed neutrals are in service, even though the rest of the system can have effectively earthed neutrals. Such systems are considered special cases and are covered in Table 21 where the TRVs specified for all test-duties are based on a k_{pp} of 1,5. For rated voltages above 170 kV, all systems and their transformers are considered to have effectively earthed neutrals.

7.105.5.5 Test-duty T10

a) For rated voltages less than 100 kV, the specified values are given in
   - Table 16 and Table 17 for class S1 circuit-breakers,
   - Table 18 and Table 19 for class S2 circuit-breakers.

b) For rated voltages of 100 kV and above, the specified standard values are given in Table 20 and Table 21. The time t_3 is a function of the natural frequency of transformers.

In case that small values of time t_3 cannot be met, the shortest time that can be met shall be used. The values used shall be stated in the test report.

7.105.5.6 Test-duties OP1 and OP2

For rated voltages up to and including 72,5 kV, the specified values are given in the following Tables.

- Table 22 for class S1 circuit-breakers for use in non-effectively earthed neutral systems;
- Table 23 for class S1 circuit-breakers for use in effectively earthed neutral systems;
- Table 24 for class S2 circuit-breakers for use in non-effectively earthed neutral systems;
- Table 25 for class S2 circuit-breakers for use in effectively earthed neutral systems.

For rated voltages of 100 kV and above, the specified values are given in Table 26 and Table 27.

Table 22 – Values of prospective TRV for out-of-phase tests on class S1 circuit-breakers for k_{pp} = 2,5

U_r	k_{pp}	k_{af}	u_c	t_3	t_d	u'	t'	u_c/t_3
kV	p.u.	p.u.	kV	µs	µs	kV	µs	kV/µs
3,6	2,5	1,25	9,19	81,4	12,2	3,06	39,3	0,113
4,76	2,5	1,25	12,1	87,4	13,1	4,05	42,2	0,139
7,2	2,5	1,25	18,4	99,7	15,0	6,12	48,2	0,184
8,25	2,5	1,25	21,1	105	15,7	7,02	50,7	0,201
12	2,5	1,25	30,6	122	18,4	10,2	59,2	0,250
15	2,5	1,25	38,3	136	20,4	12,8	65,6	0,282
15,5	2,5	1,25	39,5	138	20,7	13,2	68,6	0,287
17,5	2,5	1,25	44,7	146	22,0	14,9	70,7	0,305
24	2,5	1,25	61,2	172	25,8	20,4	83,2	0,356
25,8	2,5	1,25	65,8	179	26,8	21,9	86,4	0,368
27	2,5	1,25	68,9	183	27,5	23,0	88,5	0,376
36	2,5	1,25	91,9	214	32,1	30,6	103	0,429
38	2,5	1,25	97,0	221	33,1	32,3	107	0,440
40,5	2,5	1,25	103	229	34,3	34,5	110	0,452
48,3	2,5	1,25	123	253	37,9	41,1	122	0,488
52	2,5	1,25	133	264	39,6	44,2	128	0,503
72,5	2,5	1,25	185	329	49,3	61,7	159	0,562

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Table 23 – Values of prospective TRV for out-of-phase tests on class S1 circuit-breakers for k_{pp} = 2,0

U_r kV	k_{pp} p.u.	k_{af} p.u.	u_c kV	t_3 µs	t_d µs	u' kV	t' µs	u_c/t_3 kV/µs
3,6	2,0	1,25	7,35	65,1	9,83	2,45	31,6	0,113
4,76	2,0	1,25	9,72	69,9	10,5	3,24	33,8	0,139
7,2	2,0	1,25	14,7	79,7	12,0	4,90	38,5	0,184
8,25	2,0	1,25	16,8	83,9	12,6	5,61	40,5	0,201
12	2,0	1,25	24,5	97,9	14,7	8,16	47,3	0,250
15	2,0	1,25	30,6	109	16,3	10,2	52,5	0,282
15,5	2,0	1,25	31,6	110	16,5	10,6	53,3	0,287
17,5	2,0	1,25	35,7	117	17,6	11,9	56,6	0,305
24	2,0	1,25	49,0	138	20,6	16,3	66,4	0,356
25,8	2,0	1,25	52,7	143	21,5	17,6	69,1	0,368
27	2,0	1,25	55,1	143	22,0	18,4	70,8	0,376
36	2,0	1,25	73,5	171	25,7	24,5	82,8	0,429
38	2,0	1,25	77,6	176	26,5	25,9	85,3	0,440
40,5	2,0	1,25	82,7	183	27,4	27,6	88,4	0,452
48,3	2,0	1,25	98,6	202	30,3	32,9	97,7	0,488
52	2,0	1,25	106	211	31,7	35,4	102	0,503
72,5	2,0	1,25	148	263	39,6	49,3	127	0,563

Table 24 – Values of prospective TRV for out-of-phase tests on class S2 circuit-breakers for k_{pp} = 2,5

U_r kV	k_{pp} p.u.	k_{af} p.u.	u_c kV	t_3 µs	T_d µs	u' kV	t' µs	u_c/t_3 kV/µs
3,6	2,5	1,25	9,19	22,8	3,42	3,06	11,0	0,403
4,76	2,5	1,25	12,6	27,7	4,16	4,05	13,4	0,438
7,2	2,5	1,25	18,4	37,0	5,56	6,12	17,9	0,496
8,25	2,5	1,25	21,1	40,7	6,11	7,02	19,7	0,517
12	2,5	1,25	30,6	53,0	7,94	10,2	25,6	0,578
15	2,5	1,25	38,3	61,9	9,29	12,8	29,9	0,618
15,5	2,5	1,25	39,5	63,4	9,50	13,2	30,6	0,624
17,5	2,5	1,25	44,7	69,0	10,3	14,9	33,3	0,647
24	2,5	1,25	61,2	86,0	12,9	20,4	41,6	0,712
25,8	2,5	1,25	65,8	90,5	13,6	21,9	43,7	0,727
27	2,5	1,25	68,9	93,4	14,0	23,0	45,2	0,737
36	2,5	1,25	91,9	114	17,1	30,6	55,2	0,804
38	2,5	1,25	97,0	119	17,8	32,3	57,4	0,817
40,5	2,5	1,25	103	124	18,6	34,5	60,0	0,833
48,3	2,5	1,25	123	140	21,0	41,1	67,8	0,878
52	2,5	1,25	133	148	22,2	44,2	71,4	0,898
72,5	2,5	1,25	185	187	28,0	61,7	90,2	0,992

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Table 25 – Values of prospective TRV for out-of-phase tests on class S2 circuit-breakers for k_{pp} = 2,0

U_r	k_{pp}	k_{af}	u_c	t_3	t_d	u'	t'	u_c/t_3
kV	p.u.	p.u.	kV	µs	µs	kV	µs	kV/µs
3,6	2,0	1,25	7,35	18,2	2,74	2,45	8,82	0,403
4,76	2,0	1,25	9,72	22,2	3,33	3,24	10,7	0,438
7,2	2,0	1,25	14,7	29,6	4,44	4,90	14,3	0,496
8,25	2,0	1,25	16,8	32,6	4,89	5,61	15,8	0,517
12	2,0	1,25	24,5	42,4	6,35	8,16	20,5	0,578
15	2,0	1,25	30,6	49,5	7,43	10,2	23,9	0,618
15,5	2,0	1,25	31,6	50,7	7,60	10,6	24,5	0,624
17,5	2,0	1,25	35,7	55,2	8,28	11,9	26,7	0,648
24	2,0	1,25	49,0	68,8	10,3	16,3	33,3	0,712
25,8	2,0	1,25	52,7	72,4	10,9	17,6	35,0	0,728
27	2,0	1,25	55,1	74,4	11,2	18,4	36,1	0,737
36	2,0	1,25	73,5	91,4	13,7	24,5	44,2	0,804
38	2,0	1,25	77,6	94,9	14,2	25,9	45,9	0,817
40,5	2,0	1,25	82,7	99,3	14,9	27,6	48,0	0,833
48,3	2,0	1,25	98,6	112	16,8	32,9	54,3	0,878
52	2,0	1,25	106	118	17,7	35,4	57,2	0,898
72,5	2,0	1,25	148	149	22,4	49,3	72,1	0,992

Table 26 – Values of prospective TRV for out-of-phase tests on circuit-breakers rated for k_{pp} = 2,5 – Rated voltages of 100 kV to 170 kV

U_r	k_{pp}	k_{af}	u_1	t_1	u_c	t_2 or t_3 [a]	t_d [a]	u'	t' [a]	u_1/t_1 u_c/t_3
kV	p.u.	p.u.	kV	µs	kV	µs	µs	kV	µs	kV/µs
100	2,5	1,25	153	92	255	184-368	2-8	77	42-48	1,67
123	2,5	1,25	188	112	314	224-448	2-10	94	51-59	1,67
145	2,5	1,25	222	134	370	268-536	2-12	111	60-70	1,67
170	2,5	1,25	260	156	434	312-624	2-14	130	70-82	1,67

[a] The values of times t_2, t_d and t' indicate the lower and upper limits which should be used for testing. The time delay t_d and the time t' during testing should not be shorter than their respective lower limits and should not be longer than their respective upper limits.

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Table 27 – Values of prospective TRV for out-of-phase tests on circuit-breakers rated for k_{pp} = 2,0 – Rated voltages of 100 kV and above

U_r	k_{pp}	k_{af}	u_1	t_1	u_c	t_2 or t_3 [a]	t_d [a]	u'	t' [a]	u_1/t_1 u_c/t_3
kV	p.u.	p.u.	kV	µs	kV	µs	µs	kV	µs	kV/µs
100	2	1,25	122	80	204	160-320	2-8	61	42-48	1,54
123	2	1,25	151	98	251	196-392	2-10	75	51-59	1,54
145	2	1,25	178	116	296	232-464	2-12	89	60-70	1,54
170	2	1,25	208	136	347	272-544	2-14	104	70-82	1,54
245	2	1,25	300	196	500	392-784	2-20	150	99-117	1,54
300	2	1,25	367	238	612	476-952	2-24	184	121-143	1,54
362	2	1,25	443	288	739	576-1 152	2-29	222	146-173	1,54
420	2	1,25	514	334	857	668-1 336	2-33	257	169-200	1,54
550	2	1,25	674	438	1 123	876-1 752	2-44	337	221-263	1,54
800	2	1,25	980	636	1 633	1 272- 2 544	2-64	490	320-382	1,54
1 100	2	1,25	-	-	2 245	1 458	2-73	748	488-559	1,54
1 200	2	1,25	-	-	2 449	1 590	2-80	816	532-610	1,54

[a] The values of times t_2, t_d and t' indicate the lower and upper limits which should be used for testing. The time delay t_d and the time t' during testing should not be shorter than their respective lower limits and should not be longer than their respective upper limits.

7.105.6 Multipliers for TRV for second and third clearing poles

The TRV is defined for the first-pole-to-clear. In order to obtain the values of RRRV and u_c for the second and third clearing poles, a multiplier shall be applied to the values of RRRV and u_c of the first clearing pole at the relevant first-pole-to-clear factor. The values of these multipliers are given in Table 14.

The multipliers of Table 14 have been calculated with the assumptions given in IEC TR 62271-306 [4].

For three-phase testing the test circuit shall be designed to achieve the prospective u_c values for the second and third clearing poles. It is not necessary to meet the prospective RRRV values for the second and third clearing poles. The actual values shall be stated in the test report.

7.106 Short-circuit test procedure

7.106.1 Time interval between tests

The time intervals between individual operations of a test sequence shall be the time intervals of the rated operating sequence of the circuit-breaker, given in 5.104. For the make-break tests 7.106.3 applies. If, due to test plant limitations, the rated operating sequence cannot be achieved, the following applies:

a) The test shall be performed with the shortest achievable time interval t'. The time interval achieved shall be stated in the report. For time intervals longer than 10 min the reason for the delay shall be stated in the report;

b) For different time intervals t the following applies:

   1) t = 0,3 s: the time interval is mandatory;

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2) $t \geq 15$ s, procedure a) applies.

Prolonged time intervals shall not be due to faulty operation of the circuit-breaker.

7.106.2 Application of auxiliary power to the opening release – Breaking tests

Auxiliary power shall be applied to the opening release after the initiation of the short-circuit, but when due to test plant limitations this is impracticable the power can be applied before the initiation of the short-circuit (with the limitation that contacts shall not start to move before the initiation of the short-circuit).

7.106.3 Application of auxiliary power to the opening release – Make-break tests

In make-break tests the auxiliary power shall not be applied to the opening release before the circuit-breaker has reached the closed position. In the close-open operations of the short-circuit test-duties the power shall not be applied until at least one half-cycle has elapsed from the instant of contact touch. The close-open time shall remain as close as possible to the minimum close-open time declared by the manufacturer, but it is permissible to delay the circuit-breaker opening such that the level of asymmetry is within the permissible limit.

7.106.4 Latching on short-circuit

A circuit-breaker is latched when the main current-carrying contacts have achieved a stationary, fully engaged position at closing and this position is maintained until intentionally released, either mechanically or electrically. Unless the circuit-breaker is fitted with a making current release, or equivalent device, it shall be verified that it latches satisfactorily without undue hesitation when there is negligible decrement of the AC component of the current during the closing period.

The ability of the circuit-breaker to latch on short-circuit making current can be verified in test-duty T100s (see 7.107.5) or in the verification test for making (see 7.102.4.1). During this test the following applies:

– for three-phase tests on a three-pole circuit-breaker, the closing angle should be chosen in order to stress the pole most remote from the drive with the peak making current;

– if a single-phase test is carried out, care should be taken to stress the pole most remote from the mechanism in the same way as during a three-phase test in respect to applied voltage across the pole and current through the pole.

If the characteristics of the test plant are such that it is impossible to carry out test-duty T100s within the specified limits of the applied voltage stated in 7.105.1, the test shall be repeated at reduced voltage using a test circuit which gives the rated short-circuit making current, with negligible decrement of the AC component.

Several methods can be used to establish whether a circuit-breaker has closed and latched, for example:

– by recording of the auxiliary contacts or the contact travel;

– by visually checking the latching position after the performance of the making test;

– by recording the action of the device in order to detect latching (for example a micro-switch suitably fitted to the mechanism).

The method employed to prove satisfactory latching shall be recorded in the test report.

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