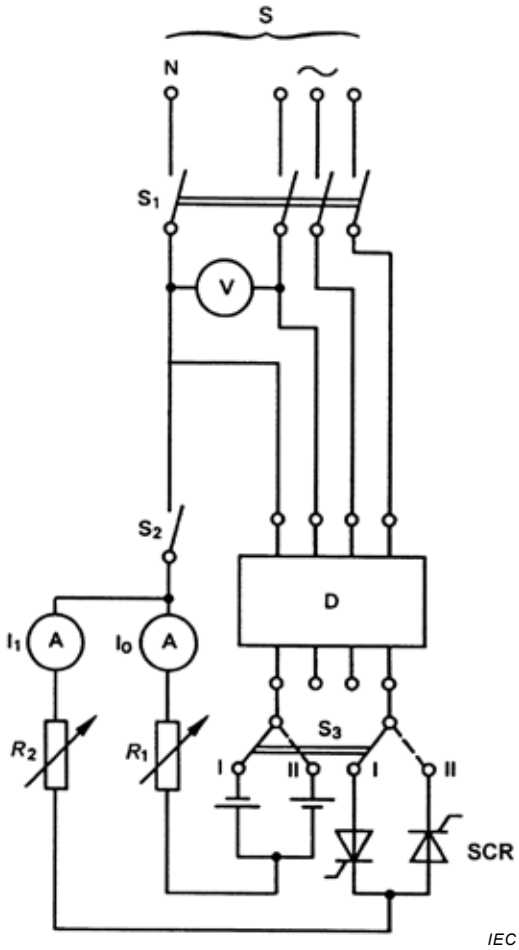

S = Supply

V = Voltmeter

A = Ammeter (measuring r.m.s values)

D = CBR under test

SCR = Thyristors

R_1, R_2 = Variable resistor

S_1 = All-pole switch

S_2 = Single pole switch

S_3 = Two-way switch

Figure B.9 – Test circuit for the verification of the correct operation of CBRs, in the case of a residual pulsating direct current superimposed by a smooth direct residual current (see B.8.7.2.4)

Annex C
(normative)

Individual pole short-circuit test sequence

C.1 General

This test sequence applies to multipole circuit-breakers intended for use on phase-earthed systems and identified in accordance with 4.3.2.1; it comprises the following tests:

Test	Clause
Individual pole short-circuit breaking capacity (I_{su})	C.2
Verification of dielectric withstand	C.3
Verification of overload releases	C.4

C.2 Test of individual pole short-circuit breaking capacity

A short-circuit test is made under the general conditions of 8.3.2, with a value of prospective current I_{su} equal to 25 % of the ultimate rated short-circuit breaking capacity I_{cu}.

NOTE Values higher than 25 % of I_{cu} can be tested and declared by the manufacturer.

The test voltage shall be the phase-to-phase voltage corresponding to the maximum rated operational voltage of the circuit-breaker at which it is suitable for application on phase-earthed systems, taking into account the requirements for recovery voltage of 8.3.2.2.6. The number of samples to be tested and the setting of adjustable releases shall be in accordance with Table 10. The power factor shall be according to Table 11, appropriate to the test current.

The test circuit shall be according to 8.3.4.1.2 of IEC 60947-1:2007/AMD1:2010 and Figure 9 of IEC 60947-1:2007/AMD1:2010, the supply S being derived from two phases of a three-phase supply, the fusible element F being connected to the remaining phase. The remaining pole or poles shall also be connected to this phase via the fusible element F.

The sequence of operations shall be

$$O - t - CO$$

and shall be made on each pole separately, in turn.

C.3 Verification of dielectric withstand

Following the test according to Clause C.2, the dielectric withstand shall be verified according to 8.3.5.4.

C.4 Verification of overload releases

Following the test according to Clause C.3, the operation of the overload releases shall be verified in accordance with 8.3.5.5.

Annex D

Vacant

Annex E
(informative)

Items subject to agreement between manufacturer and user

NOTE For the purpose of this annex

– "agreement" is used in a very wide sense;

– "user" includes testing stations.

Annex J of IEC 60947-1:2007 applies with regard to clauses and subclauses of this standard, with the following additions:

Clause or subclause number of this standard	Item
4.3.6.3	Circuit-breakers for higher short-circuit making capacity than given in Table 2
7.2.1.2.1	Automatic opening operation other than trip-free operation and by stored energy
Table 10	Setting of overload releases at intermediate values for short-circuit tests
8.3.3.5	Method of temperature-rise tests for four-pole circuit-breakers having a conventional thermal current higher than 63 A
8.3.2.6.4.3	Value of test current for short-circuit tests on the fourth pole of four-pole circuit-breakers
8.3.3.2.3, item b)	Test current value for the verification of inverse time/current characteristics
8.3.3.5	To increase the severity of the conditions for testing overload performance
8.3.3.8 8.3.4.6	Permissible delay between the verification of temperature-rise and that of overload relays in test sequences I and II
8.4.3	Calibration of releases other than over-current releases, shunt releases and undervoltage releases
8.5	Special tests – Damp heat, salt mist, vibration and shock
B.8	Applicability of tests when $I_{\Delta n}$ > 30 A
B.8.2.5	Extension of the test ambient temperature limits

Annex F
(normative)

Additional tests for circuit-breakers with electronic over-current protection

F.1 General

This annex applies to circuit-breakers intended to be installed on a.c. circuits and providing over-current protection by electronic means, incorporated in the circuit-breaker and independent of the line voltage or any auxiliary supply.

The tests verify the performance of the circuit-breaker under the environmental conditions stated in this annex.

Specific tests for electronic means intended for functions other than over-current protection are not covered by this annex. However, the tests of this annex shall be performed to ensure that these electronic means do not impair the performance of the over-current protective functions.

F.2 List of tests

F.2.1 General

Tests specified in this annex are type tests and are supplementary to the tests of Clause 8.

NOTE Where a standard for specific environmental conditions exists, reference is systematically made to this standard, if relevant.

F.2.2 Electromagnetic compatibility (EMC) tests

F.2.2.1 General

Circuit-breakers with electronic overcurrent protection shall be tested according to Table J.1 and Figure J.3.

F.2.2.2 Performance criteria

The results of immunity tests shall be evaluated on the basis of the performance criteria given in J.2.1 with the following specifications:

Performance criterion A:

For step 1, the circuit-breaker when loaded at 0,9 times the current setting shall not trip and the monitoring functions, if any, shall correctly indicate the status of the circuit-breaker.

For step 2, when loaded at 2,0 times the current setting, the circuit-breaker shall trip within 0,9 times the minimum value and 1,1 times the maximum value of the manufacturer's time current characteristic, and the monitoring functions, if any, shall correctly indicate the status of the circuit-breaker.

Performance criterion B:

During the test, the circuit-breaker when loaded at 0,9 times the current setting shall not trip. After the test, the circuit-breaker shall comply with the manufacturer's time current characteristic when loaded at 2,0 times the current setting and the monitoring functions, if any, shall correctly indicate the status of the circuit-breaker.

F.2.3 Suitability for multiple frequencies

The test shall be performed in accordance with F.6.

F.2.4 Dry heat test

The test shall be performed in accordance with F.7.

F.2.5 Damp heat test

The test shall be performed in accordance with F.8.

F.2.6 Temperature variation cycles at a specified rate of change

The test shall be performed in accordance with F.9.

F.3 General test conditions

F.3.1 General

Tests according to this annex may be performed separately from the tests of Clause 8.

In the case of the EMC tests, Annex J applies with the additional requirements specified in F.4 and F.5.

F.3.2 Electromagnetic compatibility tests

For immunity tests (F.4) one circuit-breaker per frame size and per type of current sensor design shall be tested; a change of winding turns is not considered as a different design in this context. In the case of withdrawable circuit-breaker, the device shall be mounted inside the enclosure in accordance with the manufacturer's instructions, the test set-up being modified accordingly.

The current setting I_r shall be adjusted to the minimum value.

Short-time and instantaneous release settings shall each, if applicable, be adjusted to the minimum value but to not less than 2,5 times I_r.

The tests shall be performed with the appropriate test circuit, as specified in the following subclauses, taking into account any phase-loss sensitive features.

For circuit-breakers having electronic overcurrent protection, it may be assumed that the tripping characteristics are the same, whether tests are performed:

– on individual poles of multipole circuit-breakers;
– on two or three phase poles in series;
– by three-phase connection.

NOTE This enables comparisons to be made between test results obtained on different phase pole combinations as required by the different test sequences.

For circuit-breakers incorporating a residual current function (see also Annex B and Annex M):

– in the cases of F.4.4, F.4.5 and F.4.6, tests are made on pairs of phase poles for multipole circuit-breakers, to avoid unintentional tripping by residual current;
– in the cases of F.4.1 and F.4.7, tests may be made on any combination of phase poles, as long as unintentional tripping by residual current is avoided.

F.4 Immunity tests

F.4.1 Harmonic currents

F.4.1.1 General

These tests apply to circuit-breakers for which the electronic current sensing means are stated by the manufacturer to be r.m.s. responsive.

This shall be indicated either by marking “r.m.s.” on the circuit-breaker or given in the manufacturer's literature, or both.

The EUT shall be tested in free air unless it is intended to be used only in a specified individual enclosure, in which case it shall be tested in such an enclosure. Details including the dimensions of the enclosure shall be stated in the test report.

Where applicable, the tests shall be performed at the rated frequency.

NOTE The test currents can be generated by a source of power based on the use of thyristors (see Figure F.1), saturated cores, programmable power supplies, or other appropriate sources.

F.4.1.2 Test currents

The test current waveform shall consist of one of the following two options:

– option a): two waveforms applied successively:
  - a waveform consisting of a fundamental and a third harmonic component;
  - a waveform consisting of a fundamental and a fifth harmonic component.
– option b): a waveform consisting of a fundamental and a third, fifth and seventh harmonic component.

Test currents shall be

– for option a):

  test of the third harmonic and peak factor
  - 72 % of fundamental component ≤ third harmonic ≤ 88 % of fundamental component;
  - peak factor: 2,0 ± 0,2;

  test of the fifth harmonic and peak factor
  - 45 % of fundamental component ≤ fifth harmonic ≤ 55 % of fundamental component;
  - peak factor: 1,9 ± 0,2;
– for option b):

  the test current, for each period, consists of two equal opposite half-waves defined as follows:
  - current conduction time, for each half-wave is ≤ 21 % of the period;
  - peak factor: ≥ 2,1.

NOTE 1 The peak factor is the peak value of the current divided by the r.m.s. value of the current wave. For the relevant formula, see Figure F.1.

NOTE 2 This test current for option b) has at least the following harmonic content of the fundamental component:

– third harmonic > 60 %;
– fifth harmonic > 14 %;
– seventh harmonic > 7 %;
– twenty-first harmonic > 1 %.

Other harmonics can also be present.

NOTE 3 The test current waveform for option b) can be produced by, for example, two back-to-back thyristors (see Figure F.1).

NOTE 4 The test currents 0,9 I_r and 2,0 I_r (see performance criterion A of F.2.2.2) are the r.m.s. values of the composite waveforms.

F.4.1.3 Test procedure

The tests shall be performed on two-phase poles, chosen at random in accordance with item b) of 7.2.1.2.4 carrying the test current at any convenient voltage, connections being in accordance with Figure F.2. For releases with a phase loss sensitive feature, connections shall be made in accordance with Figure F.3 or Figure F.4, as applicable.

Undervoltage releases, if any, shall either be energized or disabled. All other auxiliaries shall be disconnected during the test.

The duration of the test to verify the immunity to unwanted tripping (at 0,9 times the current setting) shall be 10 times the tripping time, which corresponds to twice the current setting.

F.4.1.4 Test results

Performance criterion A of F.2.2.2 shall apply.

F.4.2 Electrostatic discharges

Annex J, in particular J.2.2, applies with the following additions.

The test set-up shall be in accordance with Figure F.16 and Figure J.3.

The test circuit shall be in accordance with Figure F.2. For releases with a phase-loss sensitive feature, the test circuit shall be in accordance with Figure F.3 or Figure F.4, as applicable.

The busbar routing shown in Figure F.2, Figure F.3 and Figure F.4 may be varied providing the 0,1 m distances, with a tolerance of $^{+10}_{0}$ %, to the enclosure are maintained. The actual configuration used shall be shown in the test report.

Performance criterion B of F.2.2.2 applies.

F.4.3 Radiated RF electromagnetic fields

Annex J, in particular J.2.3, applies with the following additions.

The test set-up shall be in accordance with Figure F.16 and Figure F.17.

The test circuit shall be in accordance with Figure F.2. For releases with a phase-loss sensitive feature, the test circuit shall be in accordance with Figure F.3 or Figure F.4, as applicable.

Performance criterion A of F.2.2.2 applies.

F.4.4 Electrical fast transient/burst (EFT/B)

Annex J, in particular J.2.4, applies with the following additions.

The test set-up shall be in accordance with Figure F.16 and Figure F.18 for testing power lines and with Figure F.16 and Figure F.19 for testing signal lines.

On the a.c. mains port, the disturbance shall be applied on one phase pole chosen at random, the circuit-breaker being supplied from the other phase poles, in accordance with Figure F.6.

For releases which have a phase-loss sensitive feature, the test shall be performed as shown in Figure F.7 for the three phase poles in series connection or as shown in Figure F.8 on a phase pole chosen at random for the three-phase connection.

Performance criterion A of F.2.2.2 applies. However, temporary changes to the monitoring functions (e.g. unwanted LED illumination) during the tests are acceptable, in which case the correct functioning of the monitoring shall be verified after the tests. For step 2, the disturbance shall be applied until the circuit-breaker trips.

F.4.5 Surges

Annex J, in particular J.2.5, applies with the following additions.

On a.c. mains ports, the disturbance shall be applied on one phase pole chosen at random, the EUT being supplied from the other two phase poles, in accordance with Figure F.9 (line-to-earth) and Figure F.12 (line-to-line).

For releases which have a phase-loss sensitive feature, the test shall be performed as shown in Figure F.10 (line-to-earth) and Figure F.13 (line-to-line) for the three phase poles in series connection or as shown in Figure F.11 (line-to-earth) and Figure F.14 (line-to-line) on a phase pole chosen at random for the three-phase connection.

Performance criterion B of F.2.2.2 applies.

F.4.6 Conducted disturbances induced by RF fields (common mode)

Annex J, in particular J.2.6, applies with the following additions.

The test set-up shall be in accordance with Figure F.16, Figure F.20 and Figure F.21, Figure F.22 or Figure F.23 for testing power lines and with Figure F.16 for testing signal lines.

On the a.c. mains port, the disturbance shall be applied on one phase pole chosen at random, the circuit-breaker being supplied from the other phase poles, in accordance with Figure F.2.

For releases which have a phase-loss sensitive feature the test circuit shall be in accordance with Figure F.3 or Figure F.4 as applicable.

Performance criterion A of F.2.2.2 applies.

F.4.7 Current dips

F.4.7.1 Test procedure

The EUT shall be tested in free air unless it is intended to be used only in a specified individual enclosure, in which case it shall be tested in such an enclosure. Details including the dimensions of the enclosure shall be stated in the test report.

The test circuit shall be in accordance with Figure F.2 on two-phase poles chosen at random. For releases with a phase loss sensitive feature, the test circuit shall be in accordance with Figure F.3 or Figure F.4, as applicable.

The tests shall be performed with a sinusoidal current at any convenient voltage. The current applied shall be according to Figure F.5 and to Table F.1 below where I_r is the setting current, I_D is the dip test current and T is the period of the sinusoidal current.

The duration of each test shall be between three and four times the maximum tripping time corresponding to twice the current setting or 10 min, whichever is the lower.

Table F.1 – Test parameters for current dips and interruptions

Test No.	I_D	Δt
1	0	0,5 *T*
2		1 *T*
3		5 *T*
4		25 *T*
5		50 *T*
6	0,4 I_r	10 *T*
7		25 *T*
8		50 *T*
9	0,7 I_r	10 *T*
10		25 *T*
11		50 *T*

F.4.7.2 Test results

Performance criterion B of F.2.2.2 shall apply, except that the after-test verification is not required.

F.5 Emission tests

F.5.1 Harmonics

The electronic control circuits operate at very low power and hence create negligible disturbances; therefore no tests are required.

F.5.2 Voltage fluctuations

The electronic control circuits operate at very low power and hence create negligible disturbances; therefore no tests are required.

F.5.3 Conducted RF disturbances (150 kHz to 30 MHz)

Circuit-breakers covered by this annex are independent of line voltage or of any auxiliary supply. Electronic circuits have no direct coupling to the supply and operate at very low power. These circuit-breakers create negligible disturbances and therefore no tests are required.

F.5.4 Radiated RF disturbances (30 MHz to 1 GHz)

Annex J, in particular J.3.3, applies with the following additions.

The test circuit shall be in accordance with Figure F.2. For releases with a phase-loss sensitive feature, the test circuit shall be in accordance with Figure F.3 or Figure F.4, as applicable.

Undervoltage releases, if any, shall either be energized or disabled. All other auxiliaries shall be disconnected during the test.

The limits of Table J.3 apply.

F.6 Suitability for multiple frequencies

F.6.1 General

The test verifies the tripping characteristics of circuit-breakers declared as suitable for multiple frequencies. It does not apply to circuit-breakers rated at 50 Hz to 60 Hz only.

F.6.2 Test conditions

The tests shall be performed at each rated frequency or, when a range of rated frequencies is declared, at the lowest and the highest rated frequencies.

F.6.3 Test procedure

Tests shall be performed on any pair of phase-poles chosen at random at any convenient voltage.

The test circuit shall be in accordance with Figure F.2. For releases with a phase loss sensitive feature, the test circuit shall be in accordance with Figure F.3 or Figure F.4, as applicable.

Under-voltage releases, if any, shall either be energized or disabled. All other auxiliaries shall be disconnected during the test.

The short-time and instantaneous trip current settings shall each, if relevant, be adjusted to 2,5 times the current setting. If this setting is not available, the next closest higher setting shall be used.

Tests shall be performed as follows:

a) A current of 0,95 times the conventional non-tripping current (see Table 6) is applied for a time equal to 10 times the tripping time which corresponds to 2,0 times the current setting.

b) Immediately following the test of a), a current of 1,05 times the conventional tripping current (see Table 6) is applied.

c) A further test starting from the cold state is made at 2,0 times the current setting.

F.6.4 Test results

For each test frequency, the overload tripping characteristics shall comply with the following requirements:

– for test a) no tripping shall occur;

– for test b) tripping shall occur within the conventional time (see Table 6);

– for test c) tripping shall occur within 1,1 times the maximum and 0,9 times the minimum values of the manufacturer’s stated time-current characteristic.

F.7 Dry heat test

F.7.1 Test procedure

The test shall be performed on the circuit-breaker in accordance with 7.2.2 at the maximum rated current for a given frame size, on all phase poles, at an ambient temperature of 40 °C. The duration of the test, once temperature equilibrium is reached, shall be 168 h.

The tightening torques to be applied to the terminal screws shall be in accordance with the manufacturer's instructions (see 5.2 e)).

As an alternative, the test may be performed as follows: