Annex A
(normative)

Failure modes of components

The failure mode is a description of what constitutes failure for a particular component type. There are generally three types of failure – complete, partial or degraded and drift – however most data handbooks do not make this distinction, giving a total failure rate of a component that represents failure in all modes.

However information on failure modes is useful since it is the rate of occurrence of failure modes that is observed. This information is also a useful input into reliability analysis, such as diagnostics coverage, and in safety analysis in order to calculate criticality of systems.

Annex A contains details on failure modes that are useful for this purpose. These modes are higher level, usually as perceived at circuit level, than the actual physical modes that they represent and will often include within them a number of lower level modes.

The data presented herein has been derived from a number of sources such as those listed in Annex H and in IEC TR 62380. The tables give a means of allocating estimated failure rate to specific failure modes when given a specific value for total failure rate.

For prediction purposes, component failure modes can be found in Table A.1 to Table A.7.

Table A.1 – Failure modes: ICs (digital)

Environment type	Input/output fixed to 1 Stuck at U_{cc} %	Input/output fixed to 0 Stuck at ground %	Open circuit %
Stationary use at weather-protected locations E1[a]	50	50	-
Stationary use at partially weather-protected or non-weather-protected locations E2[a] Portable and non-stationary use, ground vehicle installation E3[a]	5	5	90

NOTE For digital ICs the signal pins can be defined as inputs or outputs. When a failure occurs, for each input or output pin, there are three chances:

– the (internal) failure caused the signal to be fixed at the logical level=1;

– the (internal) failure caused the signal to be fixed at logical level=0;

– the pin is no more internally connected.

The logical level=1, in terms of voltage, is usually the value of U_{cc} (positive supply voltage), while the logical level=0 is usually ground (U = 0).

Sometimes there are different voltages, hence it is more appropriate to speak in terms of stuck-at-1 or stuck-at-0 for the fixed signal at the failed pin.

For interface circuits, almost all defects are open circuits.

[a] See Table 1.

Table A.2 – Failure modes: transistors, diodes, optocouplers

		Short circuit %	Open circuit %	Drift %	Forward leakage current drift %
Transistors	Silicon	85	15		-
	GaAs	95	5		-
Diodes	Silicon	80	20		-
	GaAs	95	5		-
Zener diodes		70	20	10	
Thyristors		20	20		60
Optocouplers		10	50	40	-
Laser diodes		85	15	-	-

Table A.3 – Failure modes: LEDs

	Short circuit (forward degradation) %	Open circuit %	Optical coupling, or fibre %
Light emitting diode modules package type: with window	70	10	20
Light emitting diode modules package type: with fibre	40	10	50

Table A.4 – Failure modes: laser diodes and modules

	Diode failure %	Coupling failure %	Broken fibre %
Laser diodes modules 1,3 μm/1,55 μm modules	(degradation of the spectrum, current increase) 10	(high drop in output power) 90	-
Pump laser modules (0,98 μm 1,48 μm)	(high current increase) 90	(high drop in output power) 10	-
Modules (transmission) 0,85 μm modules (monomode fibre 9/125)	(no laser effect, degradation of the spectrum, current increase) 80	(high drop in output power) 10	(no output power) 10
Compact disks 0,85 μm modules (monomode fibre 9/125)	(no laser effect, degradation of the spectrum, current increase) 100	-	-

Table A.5 – Failure modes: photodiodes and receiver modules

	Short circuit (reverse degradation) %	Open circuit %	Coupling %
Photodiodes and receiver modules for telecommunications package type: with window	80	20	-
Photodiodes and receiver modules for telecommunications package type: with fibre	40	10	50

Table A.6 – Failure modes: capacitors

			Short circuit %	Open circuit %	Drift %
Ceramic	NPO-COG Fixed ceramic dielectric capacitors – Defined temperature coefficient – Class I		70	10	20
	X7R-X5R		90	10	-
	5ZU-Y5V-Y4T		90	10	-
	Feedthrough capacitors		70	30	-
Aluminium electrolytic	non-solid electrolyte	nominal voltage < 350 V	30	30	40
		nominal voltage > 350 V	50	-	50
	solid electrolyte		10	90	-
Tantalum electrolytic	non-solid electrolyte		80	20	-
	solid electrolyte		80	20	-
Metallized film			10	90	-
Mica			40	40	20
Variable ceramic capacitors, disks (dielectric ceramic)			40	10	50
Other technologies			10	90	-
Fixed plastic, paper, dielectric capacitors – Radio interference suppression capacitors (plastic, paper)			10	90	-
Thermistors with negative temperature coefficient (NTC)			70	10	20

Table A.7 – Failure modes: resistors, inductive devices, relays

		Open circuit %	Short circuit %	Drift %
Resistors	Carbon film	100	-	-
	Metal film	40	-	60
	High dissipation film resistors	100	0	
	Wire-wound	100	-	-
	Variable (non wirewound cermet potentiometer)	80	-	20
	Resistors network (surface mounting resistors and resistive array)	40	-	60
Inductive devices		80	20	-
Relays	General purpose	80	20	-
	Power relays	80	20	-
	Solid state relays	80	20	-
	Coaxial relays	80	20	-

Annex B
(informative)

Thermal model for semiconductors

B.1 Thermal model

This document defines the equipment ambient temperature θ_a as the average temperature around the equipment. According to IEC TR 60943 it is the air surrounding the complete device and, for devices installed inside an enclosure, it is the temperature of the air outside the enclosure.

Inside the equipment/system, there is a temperature distribution that depends on the position of the parts that dissipate power. Even if each unit in the equipment has its own temperature distribution (depending on the type of component and its position), a component ambient temperature θ_{ac} is conventionally defined, that is constant for all components in the unit, obtained by averaging the temperatures near each component. This hypothesis is generally valid for electronic units, although sometimes those that dissipate a lot of power in a single point should be excluded, in fact when a unit has areas with temperatures significantly different from θ_{ac}, for thermal modelling purposes they should be considered as two separate units.

More precisely, the component ambient temperature θ_{ac} is the temperature that would be found at the point where the component is installed supposing it could be removed (with or without heat sink). This is equivalent to supposing that there are no components that by themselves significantly influence the ambient temperature for nearby components. In other words, it is as if between each component and the others there would be a zone of separation that has a temperature equal to the component ambient temperature, that is a characteristic of the whole unit (see Figure B.1).

Situations that do not correspond to this hypothesis are handled by considering separately the parts of the unit as if they were thermally separate units, each with its own value of θ_{ac}.

Each unit inside the equipment therefore has its own thermal difference ($\Delta\theta_{a-ac}$) between the equipment ambient temperature and the component ambient temperature. This difference is assumed to be constant for each value of θ_a throughout the whole range of the latter in the range of temperatures considered normal for electric equipment, and depending on the power dissipated by the entire unit.

For all components of a unit:

$$\theta_{ac} = \theta_a + \Delta\theta_{a-ac} \tag{B.1}$$

where

θ_{ac} is the component ambient temperature (°C);

θ_a is the equipment ambient temperature (°C);

$\Delta\theta_{a-ac}$ is the difference between the equipment and component ambient temperatures (K).

In order to define or calculate the failure rate of the components, the component temperature also has to be evaluated:

$\theta_j = \theta_{ac} + \Delta\theta_{ac-j}$ junction temperature, for integrated circuits and semiconductors (B.2)

$\theta_c = \theta_{ac} + \Delta\theta_{ac-c}$ body temperature, for passive components subjected to dissipation (B.3)

In conclusion, the general thermal model can be summarized as:

$$\Delta\theta_{ac-c} = P \times R_{th,ac-j} \quad \text{(B.4)}$$

$$\Delta\theta_{ac-c} = P \times R_{th,ac-c} \quad \text{(B.5)}$$

where

P is the component power dissipation;

$R_{th,ac-j}$ is the thermal resistance between component ambient temperature and junction temperature;

$R_{th,ac-c}$ is the thermal resistance between component ambient temperature and body temperature.

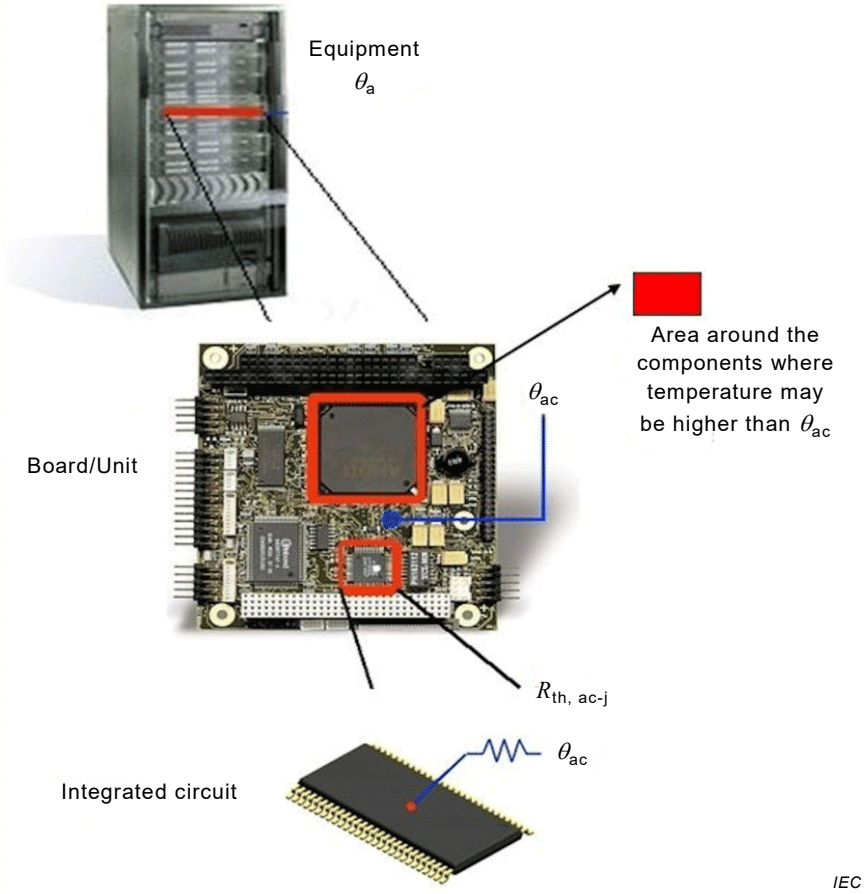

Figure B.1 – Temperatures inside equipment

B.2 Junction temperature calculation

When it is not possible to obtain the junction temperature value using the appropriate tools of the experimental thermal analysis the junction temperature value can be calculated as a function of the mean power dissipation P and of the device thermal resistance.

The simplified equation proposed here is sufficiently accurate for reliability calculations:

$$\theta_j = \theta_{ac} + P \times R_{th,\,ac-j} \quad \text{(B.6)}$$

$$\theta_j = \theta_{case} + P \times R_{th,\,c-j} \quad \text{(B.7)}$$

where

θ_j is the junction temperature (°C);

θ_{ac} is the component ambient temperature (°C);

θ_{case} is the case temperature (°C);

P is the component power dissipation (W);

$R_{th,\,ac-j}$ is the thermal resistance component ambient-junction (°C/W);

$R_{th,c-j}$ is the junction-case thermal resistance (°C/W).

B.3 Thermal resistance evaluation

The preferred method is to take the thermal resistance value specified or published by the manufacturers (see Figure B.2).

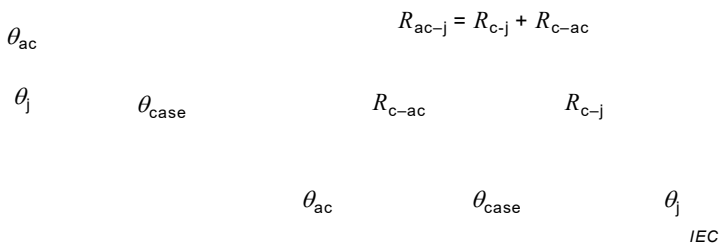

Figure B.2 – Thermal resistance model

If the device thermal resistance values are not directly available (measurements, manufacturer data), they can be calculated as a function of the package type, the pin number and the airflow factor.

Table B.1 – Thermal resistance as a function of package type, pin number and airflow factor

	$R_{th,\ c\text{-}j}$ °C/W	$R_{th,\ ac\text{-}j}$ °C/W
DIL package ceramic	$0{,}23\left(10+\frac{1520}{N+3}\right)$	$(0{,}23+0{,}66K)\left(10+\frac{1520}{N+3}\right)$
DIL package plastic	$0{,}33\left(10+\frac{1520}{N+3}\right)$	$(0{,}33+0{,}66K)\left(10+\frac{1520}{N+3}\right)$
PLCC package plastic	$0{,}28\left(15+\frac{1600}{N+3}\right)$	$(0{,}28+0{,}72K)\left(15+\frac{1600}{N+3}\right)$
SOJ and SOL package plastic	$0{,}28\left(15+\frac{1760}{N+3}\right)$	$(0{,}28+0{,}72K)\left(15+\frac{1760}{N+3}\right)$
PGA package ceramic	$0{,}33\left(10+\frac{1440}{N+3}\right)$	$(0{,}33+0{,}66K)\left(10+\frac{1440}{N+3}\right)$
QFP package plastic	$0{,}4\left(27+\frac{2260}{N+3}\right)$	$(0{,}4+0{,}6K)\left(27+\frac{2260}{N+3}\right)$
BGA package plastic	$0{,}4\left(6{,}6+\frac{1{,}1\times10^{6}}{N^{2}}\right)$	$(0{,}4+0{,}6K)\left(6{,}6+\frac{1{,}1\times10^{6}}{N^{2}}\right)$

where

N is the number of pins of the package;

K is the airflow factor given, according to the air velocity v in m/s, by the following equation

$$K=\frac{0{,}59\times v+1{,}11}{v+0{,}7} \tag{B.8}$$

where v is the air velocity in m/s. Typical values of v and K are given in Table B.2.

Table B.2 – Typical values of v are K

	v m/s	K
Natural convection	0,15	1,4
Slightly assisted cooling	0,5	1,2
Fan assisted cooling	1	1
Forced cooling	4	0,7

B.4 Power dissipation of an integrated circuit *P*

The power dissipation of an integrated circuit (where experimental values are not available) can be calculated considering its composing elements:

- a constant part from the direct current supply (P_{DC});
- a frequency dependent part (P_f);
- duty cycle, for device with standby mode (P_{stby}).

P_{DC} and P_f calculation can be performed using Table B.3:

Table B.3 – Values of P_{DC} and P_f

Type		P_{DC} W	P_f W
MOS, Bipolar, ECL, GaAs		$U_{cc\,Nom}\ I_{cc\,Max}$	0
CMOS	ACT	$1{,}6\ 10^{-3}\ U_{cc\,Nom}\ N_1$	$U_{cc}^2\ f_{op} 10^{-6}\ (C_{pd}N_2 + C_L N_3)$
	other	$U_{cc\,Nom}\ I_{cc\,Max}$ [a]	$U_{cc}^2\ f_{op} 10^{-6}\ (C_{pd}N_2 + C_L N_3)$
	memories	$U_{cc\,Nom}\ I_{cc\,Max}$	0
BICMOS		$U_{cc\,Nom}\ I_{cc\,Max}$	$U_{cc}^2\ f_{op} 10^{-6}\ (C_{pd}N_2 + C_L N_3)$

[a] Normally $P_f = 0$

where

$U_{cc\,Nom}$ is the nominal voltage (V)
(default value $U_{cc\,Nom}$ = 3 V, for BICMOS $U_{cc\,Nom}$ = 1 V to 1,8 V);

$I_{cc\,Max}$ is the maximum supply current (A);

f_{op} is the operation frequency (MHz);

C_L is the load capacitance (default value C_L = 50 pF);

C_{pd} is the power dissipation capacitance (pF);

N_1 is the number of inputs;

N_2 is the number of function elements;

N_3 is the number of outputs.

If a linear device has more than one current supply, P_{DC} is calculated separately for every supply and the values are summed.

The sum of P_{DC} and P_f, calculated in the conditions defined above, identifies the power dissipation in the worst case P_{WC} and it is a value representative of the values dispersion of different manufacturers and of different production lots.

For semi-custom integrated circuits (gate arrays and cell based), the power dissipation calculation is complex because the knowledge of the device internal composition is required, in relation to its use (registers, flip-flop and latches number).

The calculation has to be extended considering every case and it is convenient for these devices to define the maximum worst case power P_{fWC} as that one related to the maximum admitted operating frequency.

The worst case power value at the operating frequency is given by

$$P_{WC} = \frac{P_{fWC} f_{op} + P_{DC}(f_{max} - f_{op})}{f_{max}} \qquad \text{(B.9)}$$

where

P_{fWC} is the worst case power dissipation at the maximum frequency (W);

P_{DC} is the DC power dissipation (W);

f_{op} is the operating frequency (MHz);

f_{max} is the maximum operating frequency (MHz);

f_{max} = 30 MHz (HC, HCT), f_{max} = 50 MHz (AC, ACT), f_{max} = 100 MHz (BICMOS).

A conventional value of the power dissipation P_{op} to be used in the junction temperature calculation is:

$$P_{op} = P_{WC} \frac{(P_{DC} + 3{,}5)}{3 \cdot P_{WC} + 5} \quad \text{(B.10)}$$

For devices with a standby mode, particularly memories, the power dissipation P_{av} is calculated considering the duty cycle:

$$P_{av} = P_{op} \frac{D}{100} + P_{stby} \frac{(100 - D)}{100} \quad \text{(B.11)}$$

where

P_{stby} is the standby power dissipation (W);

D is the duty cycle (%).

Annex C
(informative)

Failure rate prediction

C.1 General

Reliability predictions are conducted during the whole life cycle of equipment at various levels and degrees of detail, in order to evaluate, determine and improve the dependability of the equipment.

Successful reliability prediction of equipment generally requires a model that considers the structure of the equipment. The level of detail in that model will depend on the information available at the time (e.g. parts list, circuit diagram), and several reliability models are available depending on the problem (e.g. reliability block diagrams, fault tree analysis, state-space methods).

During the conceptual and early design phase, failure rate prediction is applicable to estimate equipment failure rate in order to check if reliability targets may be achieved and to help make decisions about the architecture for the product (e.g. use of redundancy, cooling).

Reliability prediction calculations should begin as early as possible, at the start of the equipment design phase, even if not all the applicable conditions can yet be known: in this case default values can be used provisionally, to help determine those conditions which are as yet unknown. These default values will then gradually be updated as the definitive conditions are identified.

This method is far preferable to the simplified calculation method (for which all the values are replaced by default values, including those, which are already known). The calculations should therefore be prepared in such a way as to enable values to be modified easily.

The procedures in this document can be used to carry out failure rate prediction at reference and operating conditions (prediction at reference conditions is also known as part count prediction which assumes an average stress on all components, while prediction at operating conditions, also known as part stress method takes the individual load on each component into account. The part count method is usually used in the early phase of the design, while part stress prediction is used later when the detailed design has been made. For part count prediction see C.2.4.2 and for part stress see C.2.4.3.).

C.2 Failure rate prediction for assemblies

C.2.1 General

Failure rate prediction is usually performed at assembly level. Predictions are useful for several important activities in the life cycle of equipment where they are used, in addition to many other important procedures, to ensure reliability goals.

Examples of such activities:

– assess whether reliability goals can be reached;
– identify and mitigate potential design weaknesses;
– compare alternative designs;
– evaluate designs;
– provide input data for higher level assembly dependability analysis;
– conduct cost calculations (e.g. life-cycle costs);

– establish objectives for reliability tests;

– plan logistic support strategies (e.g. spare parts and resources).

Failure rate prediction is often used in combination with other tools which can be used to improve the process of prediction by making it more representative of reality by allowing assembly structure and measures of importance to be introduced.

Failure rates to be used for spare parts provisioning and life-cycle costs calculation require particular attention. For these activities, failure rates should include all causes, even design errors, equipment and dependent (pattern) failures, to provide a realistic figure of what is happening or will happen in field during the operation phase of the life cycle. See also Annex F (database).

C.2.2 Assumptions and limitations

Failure rate predictions are based on the following assumptions, resulting from focussing on physical failures occurring at random over time.

Assumptions of failure rate predictions are as follows:

– the prediction model assumes that a failure of any component will lead to a failure of the assembly;

– component failures are treated as independent of each other; no distinction is made between complete, partial and drift failures;

– components are used within their specifications;

– design and manufacturing processes of the components and assembly under consideration are under control;

– failure rates are assumed to be constant either for an unlimited period of operation (general case) or for a given limited period of interest (e.g. useful life). Although this is known to be realistic for some components for others it is not. However the assumption greatly simplifies the task;

– apart from a few exceptions the wear-out failure period is never reached by electric components; in the same way it is accepted, again apart from some exceptions, that the added risks of failure during the first few months of operation can be disregarded.

Limitations of failure rate predictions are as follows:

– they cannot provide proof that a reliability goal has been achieved;

– due to the statistical nature of the information available, prediction works best for large component and assembly counts;

– results are dependent on the trustworthiness of the source data;

– the assumption of constant component failure rates may not always be true; in such cases this method may lead to incorrect results and other models may need to be used to determine useful life;

– failure rate data and stress models may not exist for new component types;

– stresses that are not considered may predominate and influence the failure rate.

C.2.3 Process for failure rate prediction

The process for reliability prediction using failure rates consists of the following steps:

a) Define and understand the assembly to be analysed:

   – obtain information on structure, such as functional and reliability block diagrams, if available, in order to check if series assumption is valid;

   – obtain bill of materials;